Industrial Computer Source

Product Manual

Model EXM-12
Reference Manual

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FORWARD

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Technical assistance is available at (619) 271-9340.

Manual Errors, Omissions and Bugs: A Bug Sheet is included as the last page of this manual. Please use it if you find a problem with the manual you believe should be corrected.

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August 1993 New Release

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CHAPTER 1

PRODUCT DESCRIPTION

This manual contains the information you will need to install and use the EXM-12 prototyping module.

The EXM-12 is a prototyping module for use with products compatible with the EXM expansion interface. The EXM-12 printed circuit board is filled with an array of holes spaced 100 mils apart, along with hole spacing for inserting a 40-pin header at the front of the board.

It contains EXM expansion interface logic and two user-programmable PALs (part number TIBPAL20L8-15) for decoding the EXM expansion interface transactions. These PALs are socketed 24-pin PALs. The EXM-12 is shipped with these PALs installed and programmed to a default configuration.

A floppy diskette is provided with the EXM-12 containing ABEL-compatible source files for the PALs as well as an OrCAD-compatible schematic file and its archive library.

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CHAPTER 2

INSTALLATION

Before installing the EXM-12, unpack and inspect it for shipping damage.

- Do not remove the module from its anti-static bag unless you are in a static-free environment. The EXM-12, like most other electronic devices, is susceptible to ESD damage. ESD damage is not always immediately obvious. in that it can cause a partial breakdown in semiconductor devices that might not immediately result in a failure.

- Ensure that the installation process as described herein is also performed in a static-free environment.

INSERTION IN AN EXM CARRIER

Insertion of the EXM-12 into an EXM carrier is straightforward. Remove a blank EXM panel from the carrier (by unscrewing the thumbscrews) and insert the EXM-12 into the card guides. Firmly press the EXM-12 front panel to ensure that the module is properly seated in the subplane, and secure it with thumbscrews.

- Make sure that the power to your system is off. The EXM is not designed to be inserted or removed from a live system.

- When inserting the EXM, avoid touching the circuit board, and make certain the environment is static-free.

- Insert it with adequate continuous force rather than tapping or hammering on it.

CONFIGURING THE BIOS SETUP

The EXM configuration data in the EPC to which the EXM-12 is connected needs to be modified to recognize and enable the card and select from the available options. From the command line, invoke the BIOS setup function by pressing the CTRL-ALT-ESC keys simultaneously.

ENABLING THE EXM MODULE

Once in the setup program, a menu display specifying which function keys are available for further configuration. Pres the F2 function key to invoke the EXM menu. The screen display resembles Figure 1 below.

	ID	OB1	OB2
Slot 0	FF	00	00
1	DB	C1	00
2	**F3**	**05**	**00**
3	DE	00	39
4	ED	01	00
5	DC	F5	91

Figure 1. EXM Setup Screen

The setup screen displays the EXM configuration data (in hexadecimal) stored in nonvolatile memory which the EPC uses at power-up to recognize and configure each installed EXM. The displayed data shows SLOT, ID, OB1 and OB2 for each installed EXM.

Note that all slots are listed on the screen even if the actual system configuration does not have all the possible EXM slots. All slots not occupied by an EXM module should show an ID of FF and OB1/OB2 of 00. 00 indicating that no EXM is present. A typical value for the EXM-12 is shown in bold letters in slot 2.

Slot, OB1 and OB2 are defined as follows.

SLOT Indicates the slot in which the EXM is installed. See the diagram below to determine which EXM slot the EXM-12 occupies. Note that the dashed lines indicate EXM slots that may not be available on all systems.

Figure 2. EXM Slot Numbering

ID is a hard-wired ID value. Each EXM has a unique ID value.

OB1/OB2 are two bytes of option information.

To add or change an EXM configuration, use the cursor keys (arrows) to move between the fields on the screen. Move the cursor to the appropriate slot entry and type in the correct value.

The for the EXM-12 should be set to F3h.

OB1 is a hexadecimal value derived by combining the following:

Bit 7 through 4 are unused.
DMA channel 1 configured using bit 3.
The interrupt is configured using bits 2-1.
The card is enabled or disabled using bit 0.

OB2 is not used.

Bit 3 DMA Channel 1	Bits 2-1 Interrupt	Bit 0 EXM enable
0 DMA Disable 1 DMA Enable	00 none 01 IRQ9 10 IRQ5 11 IRQ15	0 Disable 1 Enable

Table 1. OB1 Setting

For instance, a typical OB1 value is 05h (00000101), representing DMA is disabled, interrupt 5 is enabled, and the EXM-12 is enabled. When selecting options, take care that there are no conflicts with other EXM modules. For instance, many of the other EXM modules have programmable interrupts and DMA channels. If more than one device is configured for a given interrupt, unstable conditions could result.

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CHAPTER 3

PROTOTYPING

PAL EQUATIONS

The EXM-12 contains three PALS, two of which are socketed DIP parts which may be replaced by the user. The EXM-12 is shipped with two installed preprogrammed PALS containing a default configuration. The third PAL, which is not user changeable, implements the EXM-12 configuration option byte register.

One socketed PAL, U1, is intended for I/O port address decode. There are two I/O address ranges: 0-3FF and 8000-83FF, U1 is connected to the following signals shown on Table 2.

Inputs	Outputs	I/Os
SA[15,9..0]	SDEN1-	IOSPARE[2..1]-
AEN	SDDIR1-	
IOR-	CS_IOX-	
IOW-	CS_IO2-	
CDEN	IOSPARE0	
ACMID-		

Table 2. U1 Signals.

Another socketed PAL, U2 is intended for memory address decode. The memory address range is 010000 - FFFFFF in 64K byte blocks. U2 is connected to the following signals.

Inputs	Outputs	I/Os
LA[23..17],SA16	MEMCS16-	MEMSPARE[4..1]-
DACK-	SDDIR-	
MEMW-	SDEN-	
MEMR-	MEMSPARE0-	
SDDIR1		
SDEN1-		
CDEN		

Table 3. U2 Signals.

Please refer to the files included on the distribution diskette for the PAL equations. For example, the file IODEC.ABL contains the following equations:

```
sddir1 = ior;
sden1 = (cden & laen & (ioadr >=^h2C0) & (ioadr <=^h2C7) & (ior # iow))
            #!aen & ior & (ioadr ==^h100) & acmid
            #(!aen & (ioadr ==^h102) & acmid & (ior # iow));
cs_IOX = !aen & (ior & (ioadr ==^h100) # (ioadr ==^h102)) & acmid;
iospare0 = cden & !aen & (ioadr ==^h2C0) & (iaodr<=^h2C7);
iospare1 = 1;
iospare2 = 2;
```

When modifying the PAL in locations U1 and U2, it is important to preserve certain mini -terms in the equations for CX_IOX, SDDIR1, SDEN1, SDDIR and SDEN. These signals control logic on the EXM-12 to enable the EXM-12 ID and option byte registers. There are specific notes in the source code that describe these issues.

DEFAULT PAL CODES

Default PAL codes do not implement the BALE signal. This signal is not necessary for I/O mapped boards, but is necessary for memory-mapped boards.

CHAPTER 4

THE EXM EXPANSION INTERFACE

The EXM Expansion Interface is used to provide local expansion of embedded PCs within the context of a larger systems architecture. Electrically, the EXM expansion interface is nearly identical to the 16-bit PC/AT Industry Standard Architecture bus (ISA bus). The difference include the following:

1. RESETDRV is negative true in the EXM expansion interface and is positive true in the ISA bus.

2. DMA channel 7, which consists of signals DRQ7 and DACK7, is not present in the EXM expansion interface.

3. The signals SA{17..19} are not present in the EXM expansion interface.

4. The addition of a signal line (EXMID) for EXM module identification.

5. The signal SBHE is negative true in the EXM expansion interface and the ISA bus. Some versions of the ISA bus documentation from IBM incorrectly define this signal as a positive true signal.

The EXMID line allows the individual expansion modules to be uniquely addressed at power-up, and facilitates software configuration as an alternative to jumpers and switches. This software configuration feature is incorporated into the EXM expansion interface in such a way that unmodified PC add-in card software can be used by EXM expansion modules. The registers that use this feature are described later in this chapter.

EXM EXPANSION INTERFACE SIGNAL DEFINITIONS AND PIN-OUT

The EXM expansion interface signals use the same names and timing as the IBM PC/AT bus signals. The only exceptions to this are the -RESETDRV signal, which is inverted in the EXM expansion interface, and the -EXMID signal, which is unique to the EXM expansion interface.

The -EXMID signal is routed to each slot and asserted by the CPU board depending on the value of register 96. In addition, the -EXMID signal is routed to each EXM slot to access the ID register (address 100H) and the programmable options select registers (addresses 102H and 103H). The -EXMID and -RESETDRV registers are used to perform module identification and configuration under software.

Refer to the *IBM Technical Reference; Personal Computer AT* document number 6139362 pages 1-31 through 1-37 for the PC/AT bus signal descriptions.

Table 4 provides the pin-out for the EXM expansion connector. The A row is on the component side of the EXM module, where it is populated with PALs, gates, and capacitors. Pin A1 is located on the bottom of the card, when the card is inserted vertically into the expansion interface with the label oriented properly. The B side of the EXM-12 is populated only with smaller resistors and capacitors.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	+12V	B1	GND	A30	-DACK5	B30	-IOR
A2	reserved	B2	reserved	A31	-DACK3	B31	-SMEMW
A3	+5V	B3	GND	A32	-DACK2	B32	-SMEMR
A4	+5V	B4	GND	A33	reserved	B33	GND

A5	SD15	B5	SD14	A34	-DACK1	B34	-MEMW
A6	SD13	B6	SD12	A35	-DACK0	B35	-MEMR
A7	SD11	B7	SD10	A36	-SBHE	B36	BALE
A8	-12V	B8	GND	A37	+5V	B37	CLK
A9	SD9	B9	SD8	A38	AEN	B38	GND
A10	SD7	B10	SD6	A39	LA23	B39	LA22
A11	SD5	B11	SD4	A40	LA21	B40	LA20
A12	+12V	B12	GND	A41	LA19	B41	LA18
A13	SD3	B13	SD2	A42	LA17	B42	SA16
A14	SD1	B14	SD0	A43	TC	B43	GND
A15	IRQ15	B15	IRQ14	A44	SA15	B44	SA14
A16	IRQ12	B16	GND	A45	SA13	B45	SA12
A17	IRQ11	B17	IRQ9	A46	key	B46	key
A18	IRQ7	B18	IRQ6	A47	key	B47	key
A19	IRQ5	B19	IRQ4	A48	SA11	B48	SA10
A20	+5V	B20	IRQ3	A49	SA9	B49	SA8
A21	-EXMID	B21	-RESETDRV	A50	OSC	B50	GND
A22	-IOCHCK	B22	GND	A51	SA7	B51	SA6
A23	DRQ6	B23	IOCHRDY	A52	SA5	B52	SA4
A24	DRQ5	B24	-0WS	A53	SA3	B53	SA2
A25	DRQ3	B25	-IOCS16	A54	SA1	B54	SA0
A26	DRQ2	B26	-MEMCS16	A55	+5	B55	GND
A27	DRQ1	B27	-REFRESH	A56	+5	B56	GND
A28	DRQ0	B28	GND	A57	reserved	B57	reserved
A29	-DACK6	B29	-IOW	A58	+12	B58	GND

Table 4. EXM Signal Pin-out.

A subset of the EXM expansion interface, along with several other useful signals, are routed to two header locations (JP3 and JP4) just in front of the card edge connector. Refer to Figure 3 on 13. These header locations can be used to wire the signals to other prototype logic that the user wishes to install. Users can either connect directly to the holes or add a header and wire wrap from these signals to the user logic. Table 4 defines the signal pin-out for these headers.

JP4				JP3	
Pin	Signal	Pin	Signal	Pin	Signal
1	SA1	29	SA0	1	SA2
2	SA4	30	SA3	2	SA5
3	SA7	31	SA6	3	OSC
4	SA9	32	SA8	4	SA10
5	SA12	33	SA11	5	SA13

6	SA15	34	SA14	6	TC
7	LA17	35	SA16	7	LA18
8	LA20	36	LA19	8	LA21
9	LA23	37	LA22	9	AEN
10	-SBHE	38	SCLK	10	BALE
11	-MEMR	39	-DACK0	11	-MEMSPARE3
12	-IOSPARE0	40	-MEMW	12	-SMEMR
13	-SMEMW	41	DRQ	13	-DACK5
14	-IOSPARE1	42	-IOR	14	-IOW
15	-IOSPARE2	43	DRQ0	15	-REFRESH
16	MEMCS16	44	USR0	16	-MEMSPARE2
17	DRQ5	45	-IOCS16	17	-0WS
18	IOCHRDY	46	USR1	18	-IOCHCK
19	-RESETDRV	47	-EXMID	19	CDEN
20	IRQ4	48	USR2	20	-MEMSPARE0
21	IRQ11	49	INT	21	-MEMSPARE1
22	-MEMSPARE4	50	USR3	22	-DACK
23	D0	51	D1	23	D3
24	D5	52	D2	24	D4
25	D6	53	D7	25	SD9
26	-12V	54	SD8	26	SD11
27	SD13	55	SD10	27	SD12
28	SD14	56	SD15	28	+12

Table 5. Prototyping Interface Connector

In the preceding table, the following signals are buffred versions of the EXM Expansion Interface signals: TC, AEN, SCLK, BALE, -SBHE, -MEMR, -MEMW, -SMEMR, -RESETDRV. The signals D0-D7 are buffered by a bi-directional buffer. The signals USR0-USR3, MEMSPARE0-MEMSPARE4, IOSPARE0-IOSPARE2, -DACK, INT, DRQ and CDEN connect to logic or spare PAL pins on the EXM-12.

The remaining signals are directly connected to the EXM expansion interface edge connector.

Note that pin 1 on the PALs and the capacitors on the JP1, JP2, JP3 and JP4 is always denoted by a squared outline around the round hole. Similarly, pin 1 on the socketed PALs is always denoted by a squared outline. Squared holes on the capacitors are +5V, while round holes are ground.

Figure 3. EXM-12 Layout.

USING THE EXM EXPANSION INTERFACE

1. For all I/O reads and writes, be sure to gate the decode with AEN deasserted. This ensures that DMA activity will not trigger an I/O access to I/O ports defined on the prototype card. Sample equations are provided on Chapter 3.

2. When generating MEMCS16, only use addresses LA17-LA23. The timing of SA0-SA16 is too late to guarantee sufficient setup time to the EXM expansion interface controller chip on the CPU board.

3. Take care when configuring the ports on the EXM-12 that the I/O addresses and memory addresses for the port do not conflict with addresses used by the CPU or other EXMs in the system. Please refer to the respective hardware reference manuals to determine potential conflicts. If there are conflicts, it is possible that permanent damage could occur to the components of the EPC or other EXM products. For instance, the EXM-12 may conflict with the EXM-

10A if one enables the EXM-10A buffer memory in the D-page. This is because the default configuration for the EXM-12 also has the D-page enabled.

4. Gate all functions on the prototype card with the CDEN signal. In other words, disable all I/O regions, memory regions, interrupt generations, and DMA usage if CDEN is not asserted.

5. When decoding both I/O and memory addresses on the EXM-12, take care that the control strobes (e.g., IOR, MEMR) are gated with any data enables to the EXM expansion interface. Otherwise, it is possible that the memory accesses can cause I/O decodes and vice versa, causing conflicts with other modules.

PROGRAMMING INTERFACE

The EXM-12 defines the following registers in the I/O space.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0	I/O port
Device ID register	1	1	1	1	0	0	1	1	100
Config Option Byte 1 Reg	User-specified				Drq	Interrupt		CDEN	102

Figure 4. EXM-12 Registers in I/O Space

Registers 100 and 102 are standard EXM registers for device identification and configuration. The EXM-12 responds to accesses to these ports only if EXM expansion interface line -EXMID is asserted. An 8-bit read from I/O address 100h returns the value F3, the device ID of the EXM-12. A read/write configuration register appears at I/O address 102h. The bit encodings are defined in Chapter 2.

User Specified bits can be used for any purpose that the user wants. These bits are read/write bits and the outputs from the register can be used to control other logic on the prototype card. These bits are available as signals USR0-USR3 as defined in Table 5 on page 11.

Drq specifies that DMA channel 1 is disabled or enabled. To use the DMA logic, the user must attach a signal to the DRQ input.

Interrupt selects the interrupt to be generated, or specifies that no interrupt is to be generated as defined in Chapter 2. To use the interrupt logic, the user must attach the interrupt source to the INT input.

CDEN specifies whether the EXM is disabled or enabled. If disabled, the EXM will not respond to any I/O or memory addresses and will not assert an interrupt output; it will only respond to reads from the I/O port 102h, and then only if -EXMID is asserted.

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