Model AV100 Technical Reference Manual

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6260 SEQUENCE DRIVE, SAN DIEGO, CA 92121 (619) 677-0877 (FAX) 619-677-0895

INDUSTRIAL COMPUTER SOURCE EUROPE *TEL (1) 69.18.74.40 FAX (1) 64.46.40.42 • **INDUSTRIAL COMPUTER SOURCE (UK) LTD** TEL 01243-533900 FAX 01243-532949*

FORWARD

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Chapter 1: About This Manual

Purpose

This technical reference manual provides technical information needed to write software for the Avanstar (AV100x) family of intelligent communications adapters from Industrial Computer Source.

Who Can Use This Manual

This manual is designed for users experienced in programming software interfaces between applications programs and communications hardware. A working knowledge of the following topics is assumed:

- Asynchronous communication protocols.
- PC architecture and operation.

Conventions Used In This Manual

This manual uses the following conventions:

- "local RAM" refers to "scratch RAM"
- "map register" refers to "latch register"
- To be consistent with programming usage, ports are numbered from 0 to 15 instead of 1 to 16.
- When discussing the dual port RAM, addresses are referenced relative to the dual port base starting address. This is because dual port RAM can be located in many different areas of memory. For example, if you select D0000H as the starting address of the dual port RAM, then the address of the Global Status Word would actually be D0002H.
- Three different numbering systems appear in this manual: binary, hexadecimal, and decimal. Each numbering system is used in its conventional context.
- Binary notation is used to represent bit values. An example is shown below.

  Bit 5 4 3 Parity Type
  x x 0 No Parity
  0 0 1 Generate and check Odd Parity.
  0 1 1 Generate and check Even Parity.
  1 0 1 Generate and check Mark Parity.
  1 1 1 Generate and check Space Parity.

- Hexadecimal notation is used to identify memory addresses and command codes. Hexadecimal numbers are always followed by "H". For example: 06H, 10H, 0AH.
- Decimal notation is used in its usual context. For example: 4 boards, 3 seconds.
- A cleared bit has a value of 0. A set bit has a value of 1.
- The term "character time" refers to the time required to transmit one character.

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Chapter 2: Overview

Introduction

The Avanstar family is a line of intelligent communication adapters that add serial ports to ISA and EISA computer systems. Each adapter has an on-board microprocessor to relieve the computer system of much of the processing necessary to support those ports. The family consists of the:

- AV100I Series for the ISA bus.
- AV100E Series for the EISA bus.

These adapters are, for the most part, functionally compatible with one another. Any differences between the adapters will be discussed in this manual.

Possible Applications

The Avanstar family adapters' versatility makes them useful for a wide range of data communication applications. For example, they may be used for data collection, process control, and interfacing to printers, scanners, modems, scales, terminals, bar code readers, burglar alarm sensors and laboratory instrumentation.

With additional programming, an Avanstar family adapter can also:

- Perform line discipline functions such as local terminal emulations and character conversions.
- Perform file-oriented algorithms such as data compacting on an interchannel basis. For example, a file can be received through one port, processed, and then re-transmitted through the same, different, or multiple ports simultaneously.
- Reconcile format differences without host computer intervention. This makes it appear as if one device is directly compatible with another system even though the actual format is different. For example, an intelligent repeater may convert ASCII to EBCDIC.

Hardware Description

The main hardware components of the Avanstar family boards are the microprocessor, QUARTs, dual ported RAM, and local RAM.

- The microprocessor is the key component of an Avanstar family board. Its main function is to transfer data from the host PC to the QUARTs, and to transfer received data from the QUARTs to the host PC. The other components of an Avanstar family board support this function.
- The QUARTs (Quad Universal Asynchronous Receiver Transmitters) are devices which convert the on-board microprocessor's parallel data into serial data for the EIA-232 interface. QUARTs also receive serial EIA-232 data and convert it to parallel data for the on-board microprocessor.
- The dual port RAM is the interface between the on-board microprocessor and the host PC.
- The local RAM is the storage location for the program that is downloaded from the host PC. The local RAM is also used for temporary data storage.

A functional diagram of the Avanstar family hardware is shown in Figure 2.1.

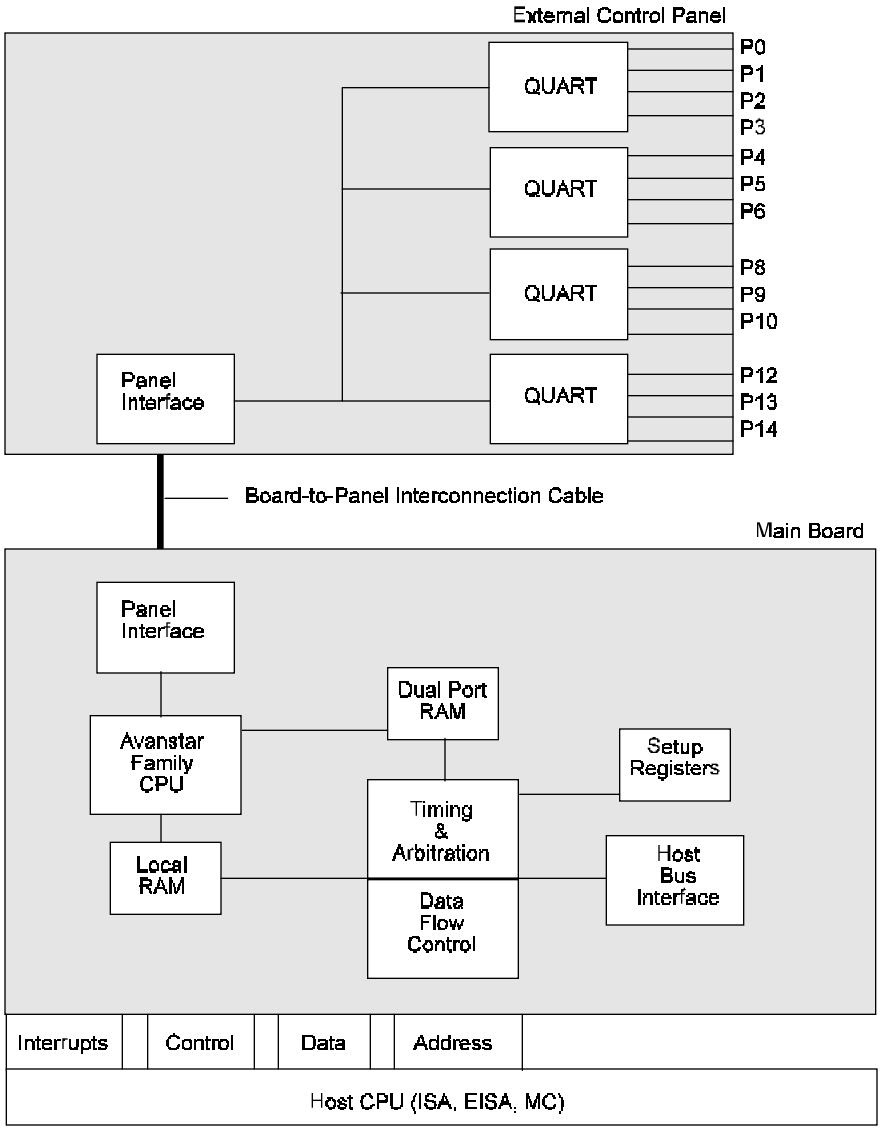


Figure 2.1 - Avanstar Family Hardware Structure.

Hardware Component Differences

The basic similarities and differences among the Avanstar family adapters are summarized in the next table. Detailed information about the adapters is given in Chapter 6.

Adapter Type	Bus	Micro Processor	Dual Port
Avanstar 100i	ISA	80186 (16MHz)	16K
Avanstar 100e	EISA	80186 (16MHz)	32K

Table 2.1 - Hardware Component Differences

There are five types of external connection panels available for all these adapters:

1. 8-port non-configurable panel
2. 8-port configurable panel
3. 16-port non-configurable panel
4. 16-port configurable panel
5. 8-channel multi-modem panel

The ports on the 8-port and the 16-port configurable panels can be software-configured as either EIA-232 or EIA-422. See the Line Protocol and Channel Command register descriptions in Chapter 4, section 4.4 for information on doing this. See your driver manual for a description of the utility which will also change the interface type.

Software Description

Three types of software enable the Avanstar family boards to function: (1) control program software, (2) host interface software, and (3) host support software.

Control Program Software

Control program software is downloaded from the host PC and executed by the on-board microprocessor. Industrial Computer Source provides standard control programs to handle communication for all boards. The information needed to write custom control program software is in Chapter 6.

Host Interface Software

Host interface software (also known as a device driver) is executed by the host PC. It transfers data from the host to the Avanstar family board, and from the Avanstar family board to the host. Various device drivers are available from Industrial Computer Source. The information needed to write custom host interface software is in Chapters 3 and 4.

NOTE:

If you are planning to support more than one type of Avanstar family adapter, it is practical to write one piece of host system software to support all types of adapters. Industrial Computer Source typically supports all adapters with the same device driver.

Host Support Software

Host support software, which is executed on the host PC, includes programs for downloading and board configuration . The information needed to write custom host support software is in Chapters 3, 4, and 5. Sample support software is provided by Industrial Computer Source on the Developer's Disk.

NOTE

If you are planning to support more than one type of Avanstar family adapter, it is practical to write one piece of host system software to support all types of adapters. Industrial Computer Source typically supports all adapters with the same device driver.

Chapter 3: Host PC Hardware Interface

Introduction

This chapter covers the Avanstar family hardware that can be accessed by the host PC.

Dual Port RAM General Information

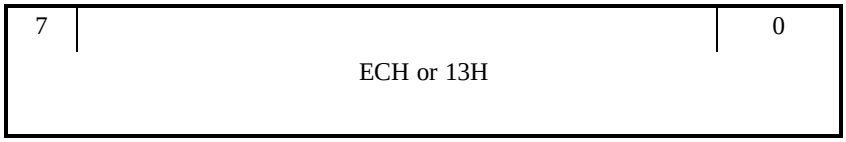
The dual port RAM is the interface between the host microprocessor and the on-board microprocessor. This memory is called dual-ported because both microprocessors can access it in order to communicate information between each other.

The dual port RAM's structure and use are determined by the software executing on the on-board microprocessor. The Avanstar family control program uses the structure and protocol defined in Chapter 4 to communicate with the host PC.

Avanstar Family ISA Bus Board

The following are the I/O registers for the ISA board.

Board ID Register (Read only) Offset:0000H



The first read after a hardware reset will be ECH. The second read will be 13H. The data will toggle between these two values on subsequent reads.

Control Register 1 Offset:0001H

7	6	5	4	3	2	1	0
IRQ Enable (Read/Write)	IRQ Select (Read/Write)			Not Used		Download Bit (Read/Write)	Program Ready Bit (Read/Write)

All bits are cleared to zero upon an ISA bus reset.

Bit 0 Program Ready Bit (Read Only)

This bit is the 80186 program ready indicator. It is cleared upon reset or download. It is set by the 80186 control program after it is downloaded and initialization is completed.

Bit 1 Download Bit (Read/Write)

This bit is tied to the 80186 reset line. Writing a one (1) to this position allows the 80186 to start executing instructions. It is usually preferable to do this after the control program has been downloaded.

Bits 6-4 IRQ Select (Read/Write)

These bits determine which ISA interrupt will be driven by the board.

Bit 6	5	4	IRQ
0	0	0	3
0	0	1	4
0	1	0	5
0	1	1	9
1	0	0	10
1	0	1	11
1	1	0	12
1	1	1	15

Bit 7 IRQ Enable (Read/Write)

This bit is used to enable the selected IRQ to be driven.

Control Register 2 Offset:0002H

7	6	5	4	3	2	1	0
186 IRQ Enable (Read/Write)	186 IRQ Data (Read/Write)	Not Used	Memory Enable (Read/Write	Memory Bank Select Bits (Read/Write)			

All bits are cleared to zero upon an ISA bus reset.

Bits 3-0 Memory Bank Select Bits (Read/Write)

These bits are used to select the correct 16K memory bank from either the dual port or the local RAM as applicable. During download, the two low order bits of this register correspond to the two high order bits of the local RAMs.

Bit 4 Memory Enable (Read/Write)

This bit determines if the board responds to any ISA memory cycles. When in download mode, this bit controls the local RAM response to ISA memory cycles. When not in download mode, this bit controls the dual port RAM response to ISA memory cycles.

Bit 6 186 IRQ Data (Read Only)

This bit reflects the current state of the 80186 IRQ data bit which is toggled by the control program. See section 6.5—80186 register PCS1.

Bit 7 186 IRQ Enable (Read Only)

This bit reflects the current state of the 80186 IRQ enable bit which is toggled by the control program. See section 6.5—80186 register PCS1.

ISA Bus Dual Port Address Register (R/W) Offset:0003H

7	6	5	4	3	2	1	0
Address Line A19	Address Line A18	Address Line A17	Address Line A16	Address Line A15	Address Line A14	Not Used	

All bits are cleared to zero upon an ISA bus reset.

Bits 7-2 Address Lines A19-A14

These bits select address lines A19-A14 for the base address of the dual port RAM 16K byte window.

ISA Bus Board Interrupt Status Register 1 Offset:0004H

7	6	5	4	3	2	1	0
Channel 8	Channe 7	Channe 6	Channel 5	Channel 4	Channel 3	Channel 2	Channel 1

This register gives the pending interrupt status for channels 1-8. The register is read only from the ISA bus and write only from the 80186. The bits are cleared when there is a reset, an ISA bus read, or when the Download Bit in Control Register 1 is low. This register is not used by the standard Avanstar family control program.

ISA Bus Board Interrupt Status Register 2 Offset:0005H

7	6	5	4	3	2	1	0
Channel 16	Channe 15	Channe 14	Channel 13	Channel 12	Channel 11	Channel 10	Channel 9

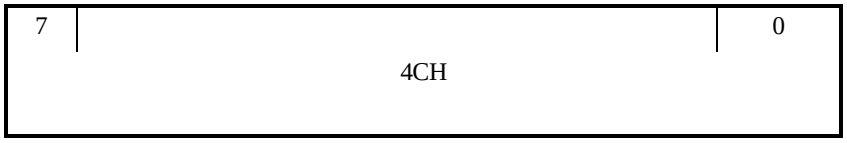
This register gives the pending interrupt status for channels 9-16. The register is read-only from the ISA bus and write-only from the 80186. The bits are cleared when there is a reset, an ISA bus read, or when the Download Bit in Control Register 1 is low. This register is not used by the standard Avanstar family control program.

Avanstar Family EISA Bus Board

The Avanstar EISA board uses EISA slot-specific I/O registers. They are located from xC80H through xCAEH, where x is the EISA slot number in hexadecimal. For example, if an Avanstar EISA board is installed in slot 1, its registers would be located at I/O addresses 1C80H through 1CAEH.

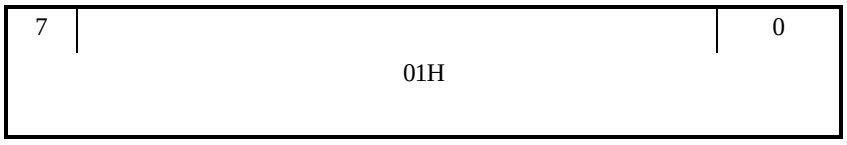
EISA Bus Board ID Registers (Read only) I/O Address: xC80H-xC83H

Register at I/O Address xC80H

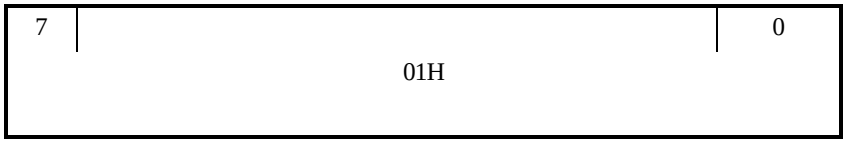


Register at I/O Address xC81H

Register at I/O Address xC82H



Register at I/O Address xC83H



These registers contain the four-byte EISA Board ID.

Board Control Register I/O Address: xC84H

7	6	5	4	3	2	1	0
Reserved (0)					IOCHKRST (write only)	IOCHKRS (Read only)	ENABLE (Read/Write)

This register contains the ENABLE, IOCHKERR, and IOCHKRST bits defined in the EISA specification.

Bit 0 Enable (Read/Write)

Setting this bit to 1 enables the board for operation. Clearing this bit to 0 disables operation of the board and causes it to respond only to slot-specific I/O. This bit is cleared to 0 on reset and when the IOCHKRST bit is pulsed.

Bit 1 IOCHKERR (Read Only)

This bit is set to 1 to indicate a serious error. This bit is cleared to 0 on reset and when the IOCHKRST bit is pulsed.

Bit 2 IOCHKRST (Write Only)

This bit is cleared to 0 for normal operation. Pulse this bit to 1 for at least 500 ns to reset the board. Pulsing this bit disables the board and clears the ENABLE and IOCHKERR bits.

Map Registers I/O Addresses: xC85H-xC87H

Register at I/O Address xC85H

7	6	5	4	3	2	1	0
Address Line A15	Address Line A14	Address Line A13	Address Line A12	Address Line A11	Address Line A10	Always 0	Alway 0

Register at I/O Address xC86H

7	6	5	4	3	2	1	0
Address Line A23	Address Line A22	Address Line A21	Address Line A20	Address Line A19	Address Line A18	Address Line A17	Addres Line A16

Register at I/O Address xC87H

7	6	5	4	3	2	1	0
Address Line A31	Address Line A30	Address Line A29	Address Line A28	Address Line A27	Address Line A26	Address Line A25	Addres Line A24

These registers select address lines A31-A10 for the dual port RAM.

EISA Bus Board Dual Port Mode Register I/O Address: xCA1H

7		0
Dual Port Mode		

This register determines the mode of operation of the dual port RAM. Before accessing the dual port RAM while in Download Mode, this register must be set to 4EH. Before accessing the dual port RAM in the Normal Operating Mode, this register must be set to 6EH.

EISA Bus Board Interrupt Select Register I/O Address: xCA8H

7		0
Undefined		Interrupt Select

This register is used in conjunction with the Interrupt Configuration and Status Register to determine which IRQ level the board uses. See the Interrupt Level Bits of the Interrupt Configuration and Status Register for use of this register. The Interrupt Select bit is reset to 0 after a hardware reset.

EISA Bus Board Interrupt Configuration and Status Register I/O Address: xCA9H

7	6	5	4	3	2	1	0
Interrupt Pending	Reserved	Always 0	Always 1	Interrupt Enable	Reserved	Interrupt Level	

This register, in conjunction with the Interrupt Select Register, determines the configuration of interrupts of the board. Reading this register reports the interrupt status of the board and also clears the interrupt. Interrupt service routines must read this register at the start of their processing to clear the interrupt.

Bits 1-0 Interrupt Level

These bits, in conjunction with the Interrupt Select Bit of the Interrupt Select Register, determine which IRQ level the board uses.

Interrupt	Bit		
Select Bit	1	0	IRQ Level
0	0	0	IRQ 3
0	0	1	IRQ 4
0	1	0	IRQ 5
0	1	1	IRQ 9
1	0	0	IRQ 10
1	0	1	IRQ 11
1	1	0	IRQ 12
1	1	1	IRQ 15

Bit 3 Interrupt Enable

Setting this bit to 1 enables interrupts from the board. Clearing this bit to 0 disables interrupts from the board.

Bit 7 Interrupt Pending

This bit is set to 1 when an interrupt is pending. This bit is cleared to 0 when there is not an interrupt pending. This bit is reset to 0 after this register is read.

EISA Bus Board Status Register I/O Address: xCACH

7		0
	Undefined	Board Ready

This register returns the status of the board.

Bit 0 Board Ready

This bit is set to 1 when the processor sets its ready bit. This bit is cleared to 0 when the processor has not set its ready bit. This bit is reset to 0 when the board is placed in reset or in the download mode.

EISA Bus Board Download Register I/O Address: xCADH

7		2	1	0
Undefined			Local RAM Bank Select	Board Ready

This register controls the board mode and selects the local RAM block in the download mode.

Bit 0 Download Mode

Clearing this bit to 0 places the board in the download mode. This holds the processor in the reset state and forces the local RAM to overlay the dual port RAM for the download operation. Setting this bit to 1 sets the main board and processor to normal operation.

Bit 1 Local RAM Bank Select

The Avanstar EISA board has 64KB of local RAM, but there is only a 32KB window to the host. This bit selects which block of the local RAM is mapped to the host's window.

Clearing this bit to 0 selects the lower local RAM block (0000H - 7FFFH). Setting this bit to 1 selects the upper local RAM block (8000H - FFFFH).

EISA Bus Board Dual Port Enable Register I/O Address: xCAEH

7	6	5	4	3	2	1	0
Always 0			Dual Port Enable	Always 0			

This register enables and disables the dual port RAM.

Bit 4 Dual Port Enable

Setting this bit to 1 enables the dual port RAM. Clearing this bit to 0 disables the dual port RAM.

NOTE:

Please refer to the Hitachi HD6498IF EISA Slave Interface Controller data sheet (available from your local Hitachi rep) for a further description of these registers.

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Chapter 4: Avanstar Family Control Program

Introduction

The Avanstar family control program is the standard control program software provided by Industrial Computer Source. It contains the code necessary to carry out the main functions of the Avanstar family: transmitting and receiving data.

Each type of Avanstar family adapter has a separate but functionally compatible control program. The following table lists the Avanstar family adapters with their control program filenames.

Board Type	Control Program Filename
Avanstar 100i	A100I.CP
Avanstar 100e	A100E.CP

The Avanstar family Developer's disk contains the DOS utility program A100LOAD.EXE that will download a control program to any Avanstar family board. The source code for A100LOAD.EXE is also contained on the Avanstar family developer's disk.

Dual Port RAM Interface

The Avanstar family control program and the host interface program communicate through the dual port RAM. This chapter describes the structure of this interface and its theory of operation.

The Avanstar family control program logically divides the dual port RAM into three sections:

- Global Control Block
- Channel Control Blocks
- Buffer Area

Global Control Block

The Global Control Block (GCB) is the section of the dual port memory which contains command fields and data which apply to the Avanstar family board in general. Table 4.1 lists the fields making up the Global Control Block.

GCB Offset	Field Description	Access
0000H	Global Command Word	(R/W)
0002H	Global Status Word	(RO)
0004H	Global Service Request	(X)
0006H	Available Buffer Space Remaining	(RO)
0008H	Board Type	(RO)
000AH	Avanstar Family Control Program Version	(RO)
000CH	Channel Control Block Count	(RO)
000EH	Channel Control Block Offset	(RO)
0010H	Channel Control Block Size	(RO)
0012H	Global Command Word 2	(R/W)
0014H	Global Status Word 2	(RO)
0016H	Communication Error Service Request	(X)
0018H	Input Buffer Service Request	(X)
001AH	Output Buffer Service Request	(X)
001CH	Modem Status Change Service Request	(X)
001EH	Channel Command Service Request	(X)

TABLE 4.1 - Global Control Block Fields

NOTES

1. Offsets are from the base address of the Global Control Block. The base address of the Global Control Block is the same as the base address that was selected for the dual-port RAM.

2. The different access types are:

   (RO) Read Only
   (R/W) Read and Write
   (X) Exchange

   The fields with an access type of (X) are Service Request fields.

Global Command Word (R/W) GCB Offset: 0000H

The host interface program uses the Global Command Word to issue commands to the Avanstar family control program. Write the desired command to this field, wait for the field to return to 0000H, and then check the Global Status Word for any errors.

Global Command 0000H: Ready

After the Avanstar family control program has been downloaded and its initialization has been completed, the program enters the Normal Operating Mode and writes a 0000H to the Global Command Word. In this mode, characters can be transmitted and received, channels can be configured, and commands can be issued to the Avanstar family control program.

Global Command 0001H: Diagnostic Mode

Diagnostic Mode is not currently implemented by the Avanstar family control program.

Global Command 0002: Reset

Reset stops the Avanstar control program and restarts the resident firmware. This command deletes the Avanstar family control program from the local RAM and prepares the adapter for another download. This is a software-only reset; no hardware is reset by this command.

Global Status Word (RO) GCB Offset: 0002H

The host interface uses the Global Status Word to find out the current status of the Avanstar family control program and related hardware.

Global Status 0000H: Ready

Ready means that the Avanstar family control program is in the Normal Operating Mode and that no errors have occurred.

Global Status 0001H: Stopped

Stopped means that the Avanstar family control program has stopped because of an unexpected error.

Global Status 0002: Dual Port RAM Error

Dual Port RAM Error means that the Avanstar family control program detected an error in the dual port memory during initialization.

Global Status 0003H: Invalid Command

Invalid Command means that an invalid command was placed in the Global Command Word.

Global Status 0004H: Busy

Busy is placed in the Status Word by the Avanstar family control program while it is initializing. After it has initialized, the Avanstar family control program enters the Normal Operating Mode and places a 0000H in the Status Word to indicate that it is ready.

Global Service Request (X) GCB Offset: 0004H

7	6	5	4	3	2	1	0
Channel 7	Channe 6	Channe 5	Channel 4	Channel 3	Channel 2	Channel 1	Channel 0

15	14	13	12	11	10	9	8
Channel 15	Channe 14	Channe 13	Channel 12	Channel 11	Channel 10	Channel 9	Channel 8

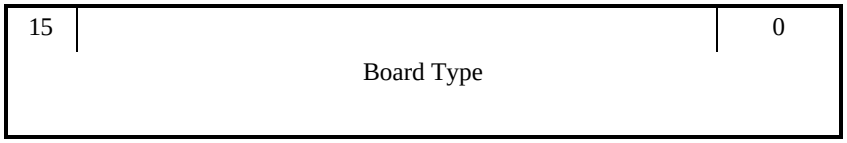
The Global Service Request is used to indicate the channels which request service. Each time any of the five service request conditions occur, the bit corresponding to the channel is set.

For all eight-port boards, bits 15-8 are always cleared to 0.

Available Buffer Space Remaining (RO) GCB Offset: 0006H

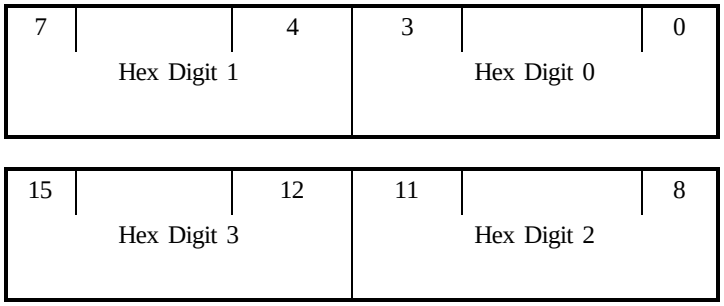
This field shows the amount of buffer space available for input and output buffers. The Available Buffer Space Remaining field is updated after each configuration.

Board Type (RO) GCB Offset: 0008H



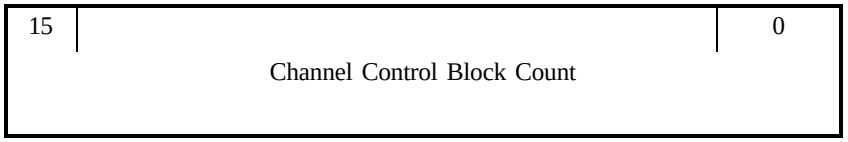
Value	Board Type
0006H	Avanstar 100m
000AH	Avanstar 100e
000CH	Avanstar x00i

Avanstar Control Program Version (RO) GCB Offset: 000AH



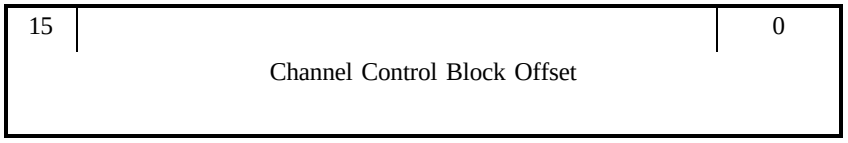
This field shows the Avanstar family control program version in use. The version level is encoded into the field as follows: version WX.YX is encoded as WXYZH, where W, X, Y and Z represent hexadecimal digits. For example, version 4.56 would be encoded as 0456H.

Channel Control Block Count (RO) GCB Offset: 000CH



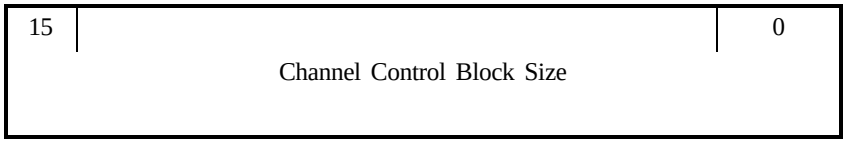
This field shows the number of channel control blocks set up by the control program. This number reflects the number of ports (8 or 16) on the external connection panel.

Channel Control Block Offset (RO) GCB Offset: 000EH



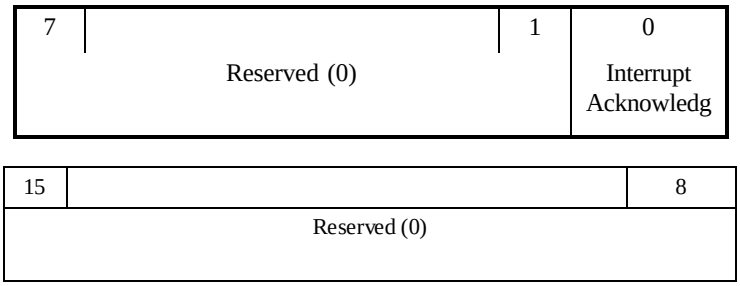
This field contains the offset of the first Channel Control Block (CCB) from the base of the dual ported memory. This is necessary because future revisions may change the size of the GCB. Use this field to determine the base address of the first CCB.

Channel Control Block Size (RO) GCB Offset: 0010H



This field contains the size of each Channel Control Block (CCB). This is necessary because future revisions may change the size of the CCB. Use this field to determine the base addresses of the remaining CCBs.

Global Command Word 2 (R/W) GCB Offset: 0012H

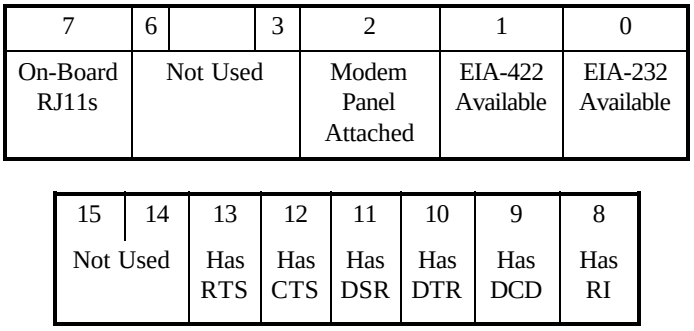


The Global Command Word 2 is used by the application to give additional commands to the control program.

Bit 0 Interrupt Acknowledge

Setting this bit to "1" informs the Avanstar family control program that the host interface program is ready to accept interrupts. This bit is set only once.

Global Status Word 2 (RO) GCB Offset: 0014H



The Global Status Word 2 field contains a unique ID which describes what type of external connection panel is installed. The ID is read by the control program at power-up and is made available to the driver.

NOTE:

A value of 0000H in this field indicates either that no external connection panel is installed, or a non-Avanstar family external connection panel is installed.

Bit 7 On-Board RJ11s

This board has RJ type connectors on it-no panel is attached.

Bits 8-13

This adapter supports the indicated handshake signals. (1=supported)

Communication Error Service Request (X) GCB Offset: 0016H

7	6	5	4	3	2	1	0
Channel 7	Channel 6	Channel 5	Channel 4	Channel 3	Channel 2	Channel 1	Channel 0

15	14	13	12	11	10	9	8
Channel 15	Channel 14	Channel 13	Channel 12	Channel 11	Channel 10	Channel 9	Channel 8

This field is used to inform the host interface program which channels require servicing due to communication errors. The bit corresponding to the requesting channel is set each time a break is received or an overrun error, parity error, or framing error occurs.

For all eight-port boards, bits 15-8 are always cleared to 0.

Input Buffer Service Request (X) GCB Offset: 0018H

7	6	5	4	3	2	1	0
Channel 7	Channel 6	Channel 5	Channel 4	Channel 3	Channel 2	Channel 1	Channel 0

15	14	13	12	11	10	9	8
Channel 15	Channel 14	Channel 13	Channel 12	Channel 11	Channel 10	Channel 9	Channel 8

This field is used to inform the host interface program which channels require servicing due to an input buffer condition. The bit corresponding to the requesting channel is set each time one of these conditions occur:

- The number of characters specified by the trigger rate has been received.
- The most recent character was received more than 4 character times in the past.
- The input buffer fills up.

For all eight-port boards, bits 15-8 are always cleared to 0.

Output Buffer Service Request (X) GCB Offset: 001AH

7	6	5	4	3	2	1	0
Channel 7	Channel 6	Channel 5	Channel 4	Channel 3	Channel 2	Channel 1	Channel 0

15	14	13	12	11	10	9	8
Channel 15	Channel 14	Channel 13	Channel 12	Channel 11	Channel 10	Channel 9	Channel 8

This field is used to inform the application program which channels require servicing due to an output buffer condition. The bit corresponding to the requesting channel is set each time the output buffer is empty or at the low water mark.

For all eight-port boards, bits 15-8 are always cleared to 0.

Modem Status Change Service Request (X) GCB Offset: 001CH

7	6	5	4	3	2	1	0
Channel 7	Channel 6	Channel 5	Channel 4	Channel 3	Channel 2	Channel 1	Channel 0

15	14	13	12	11	10	9	8
Channel 15	Channel 14	Channel 13	Channel 12	Channel 11	Channel 10	Channel 9	Channel 8

This field is used to inform the application program which channels require servicing due to a modem status change. The bit corresponding to the requesting channel is set each time the modem status changes.

For all eight-port boards, bits 15-8 are always cleared to 0.

Channel Command Service Request (X) GCB Offset: 001EH

7	6	5	4	3	2	1	0
Channel 7	Channe 6	Channe 5	Channel 4	Channel 3	Channel 2	Channel 1	Channel 0

15	14	13	12	11	10	9	8
Channel 15	Channe 14	Channe 13	Channel 12	Channel 11	Channel 10	Channel 9	Channel 8

This field is used to inform the application program which channels require servicing due to the completion of a channel command. The bit corresponding to the requesting channel is set each time a channel command is completed successfully or unsuccessfully.

For all eight-port boards, bits 15-8 are always cleared to 0.

Channel Control Blocks

The Channel Control Blocks (CCB) are subdivided into fields which reflect the status of a particular channel. CCBs contain channel-specific data and command words. Certain CCB fields can cause the Avanstar family board to perform specific operations. There is one CCB for each of the channels supported by the board.

Since future revisions of the Avanstar family control program may enlarge the size of the GCB or CCBs, we have devised a method to make upgrading the control program easier. Currently defined fields will always remain fixed relative to the base of their control blocks. Any field added in the future will be added after the current ones.

In the GCB, the Channel Control Block Offset field contains the offset of the first Channel Control Block from the base of the dual port RAM. Use this field to determine the base address of the first CCB. The Channel Control Block Count field of the GCB contains the number of Channel Control Blocks set up by the Avanstar family control program.

The Channel Control Block Size field of the GCB contains the size of each Channel Control Block. Use this field to determine the base addresses of the remaining CCBs.

After downloading, a set of default configuration parameters is established. The CCB default parameter values are:

Baud Rate	9600	
Bits Per Character	8	
Number of Stop Bits	1	
Parity Type	None	
Line Protocol	None	
Input or Output	976	Avanstar 100e (16 ports)
Buffer Size	2000	Avanstar 100e (8 ports)
	464	Avanstar 100m, x00i (16 ports)
	976	Avanstar 100m, x00i (8 ports)
Input Buffer Trigger Rate	0 (Every Character)	
Output Buffer Low Water	0 (Empty)	
Input Buffer High Water	944	Avanstar 100e (16 ports)
	1968	Avanstar 100e (8 ports)
	432	Avanstar 100m, x00i (16 ports)
	944	Avanstar 100m, x00i (8 ports)
Input Buffer Low Water	912	Avanstar 100e (16 ports)
	1936	Avanstar 100e (8 ports)
	400	Avanstar 100m, x00i (16 ports)
	912	Avanstar 100m, x00i (8 ports)

TABLE 4.2 - Channel Control Block Default Parameters

CCB Offset	Field Description	Access
0000H	Baud Rate	(R/W)
0002H	Data Format	(R/W)
0004H	Line Protocol	(R/W)
0006H	Input Buffer Size	(R/W)
0008H	Output Buffer Size	R/W)
000AH	Input Buffer Trigger Rate	(R/W)
000CH	Output Buffer Low Water Mark	(R/W)
000EH	IXON Characters	(R/W)
0010H	Input Buffer High Water Mark	(R/W)
0012H	Input Buffer Low Water Mark	(R/W)
0014H	Channel Command	(R/W)
0016H	Channel Status	(R/W)
0018H	Input Buffer Starting Address	(RO)
001AH	Input Buffer Ending Address	(RO)
001CH	Output Buffer Starting Address	(RO)
001EH	Output Buffer Ending Address	(RO)
0020H	Next Character to Input Buffer	(RO)
0022H	Next Character from Input Buffer	(R/W)
0024H	Next Character to Output Buffer	(R/W)
0026H	Next Character from Output Buffer	(RO)
0028H	Communication Error Status	(X)
002AH	Bad Character Pointer	(R/W)
002CH	Modem Control	(R/W)
002EH	Modem Status	(RO)
0030H	Blocking Status	(RO)
0032H	Character Received Flag	(R/W)
0034H	IXOFF Characters	(R/W)
0036H	Channel Status 2	(RO)

TABLE 4.3 - Control Program Channel Control Block Definition

NOTES

1. Offsets are from the base of the specific Channel Control Block.
2. The different access types are:

   (RO) Read Only
   (R/W) Read and Write
   (X) Exchange

The field with an access type of (X) is the Communication Error Status field. This field must be updated by both the host PC and the Avanstar family processor. To avoid the possibility of losing a Communication Error Status bit, the host PC must access and clear the field using the XCHG (assembler) instruction with the register operand cleared to zero.

Baud Rate (R/W) CCB Offset: 0000H

This field defines a baud rate for the receiver and transmitter in the corresponding Avanstar family board channel.

The following baud rates can be selected on each channel for all Avanstar family boards:

50	300	4800	57600
75	600	7200	64000
110	1050	9600	76800
134.5	1200	19200	115200
150	1800	38400	
200	2400	56000	

TABLE 4.4 - Available Baud Rates

NOTES

1. Because decimal values can not be directly represented in the Baud Rate field, it is necessary to use the value 134 in the field in order to program the baud rate 134.5.
2. Because the baud rate is stored as an unsigned word value in this field, the highest value that can be represented directly is 65535. Due to this limitation, it is necessary for the control program to perform a translation for some of the higher baud rates. Use the following table to program higher baud rates:

Actual Baud Rate	Baud Rate Field Value in CCB
76800	FF00H
115200	FF01H

Data Format (R/W) CCB Offset: 0002H

7	6	5	4	3	2	1	0
Channel Mode		Parity Type			Number of Stop Bits	Number of Data Bits	

15	6	9	8
Reserved (0)		Error Reporting Type	

This field defines the number of data bits, number of stop bits, parity type, and channel mode of the corresponding channel.

Bits 1-0 Number of Data Bits

Defines the number of data bits in each transmitted or received character.

Bit		Number of Data Bits
	0 0	5 Bits
	0 1	6 Bits
	1 0	7 Bits
	1 1	8 Bits

Bit 2 Number of Stop Bits

Clearing to “0” generates and checks 1 stop bit.

Setting “1” generates and checks 2 stop bits.

Bits 5-3 Parity Type

Defines the parity generated and checked.

Bit		Parity Type
	x x 0	No Parity
	0 0 1	Generate and Check Odd Parity
	0 1 1	Generate and Check Even Parity
	1 0 1	Generate and Check Mark Parity
	1 1 1	Generate and Check Space Parity

Bits 7-6 Channel Mode

Each channel can operate in one of four modes.

Bit		Mode
	0 0	Normal
	0 1	Automatic Echo (Not supported on Avanstar 100m)
	1 0	Local Loopback
	1 1	Remote Loopback

- In the Normal mode, the transmitter and receiver operate independently.
- In the Automatic Echo mode, received data is retransmitted. Received data is sent to the Avanstar family processor, but the Avanstar family CPU-to-transmitter link is disabled.
- In the Local Loopback mode, the transmitter is internally connected to the receiver. The transmitter output is held in the mark state.
- In the Remote Loopback mode, received data is retransmitted. Received data is not sent to the Avanstar family processor, and the Avanstar family CPU-to-transmitter link is disabled.

Bit 8 Error Reporting Type

Clearing this bit to 0 causes the control program to report communication errors and to place a value of FFH in the dual port input buffer as described in section 4.5.3. Setting this bit to 1 causes the control program to report communication errors and to place the actual character received in the dual port input buffer as described in section 4.5.3 .

Bits 15-9 Reserved (0)

These bits are always cleared to 0.

Line Protocol (R/W) CCB Offset: 0004H

7	6	5	4	3	2	1	0
Enable Modem Control/Status	Input Buffer Controls RTS	Transmitter Controls RTS	Receiver Controls DTR	CTS Controls Transmitter	IXOFF	IXANY	IXON

15	14	13	12	11	10	9	8
Reserved (0)		Interface Type	Character Strip Enable	Reserved (0)			

This field defines the line protocol used for the UART.

Bit 0 IXON

This bit enables start/stop output control. When the Avanstar family adapter receives the XOFF character, it stops sending data on that channel until the XON character is received. Then transmission is resumed.

To select the XON/XOFF characters for control, place the hex codes of the desired characters in the upper and lower byte of the IXON Characters field of the CCB.

Bit 1 IXANY

Use of this protocol requires that IXON also be enabled. When the Avanstar family adapter receives the XOFF character, it stops sending data on that channel. Once transmission is suspended, any character received on that channel will cause character transmission to resume if this bit is set.

As with the IXON protocol, place the XON/XOFF characters used for control in the IXON Characters field. If none are specified, the default is XON = 11H and XOFF = 13H.

Bit 2 IXOFF

Setting this bit transmits start/stop characters. When the input buffer reaches the mark set by the Input Buffer High Water Mark field, the character defined as XOFF is transmitted. This signals the remote device to stop sending characters. After the input buffer level is emptied to below the value set by the Input Buffer Low Water Mark, the character defined as XON is transmitted. This signals the remote device to resume sending characters.

To select the XON/XOFF characters for control, place the hex codes of the desired characters in the upper and lower byte of the IXOFF Characters field. If none are specified, the default is XON = 11H and XOFF = 13H.

Bit 3 CTS Controls Transmitter

Setting this bit specifies that the transmitter will respond to the state of the CTS handshake line. This function is implemented in the UART hardware. When the CTS line is asserted, the transmitter is enabled to transmit characters. When the CTS line is negated, the transmitter is disabled and will not transmit any characters.

Bit 4 Receiver Controls DTR

Setting this bit specifies that the UART hardware controls the DTR line. DTR is always asserted, except when the UART input FIFO fills up. The blocking status is not updated by this protocol.

If Modem Control/Status is enabled, the DTR bit in the Modem Control field of the CCB must be set for this protocol to assert DTR.

NOTE

It may appear that the receiver controls RTS instead of DTR. However, this is only because the external connection panel's RTS and DTR lines have been switched.

Bit 5 Transmitter Controls RTS

Setting this bit specifies that the transmitter will control the RTS handshake line. Setting this bit causes the RTS line to be negated automatically one bit time after the characters in both the transmitter shift register and the holding register are completely transmitted.

Bit 6 Input Buffer Controls RTS

Setting this bit specifies that the receiver will control the RTS handshake line. When this protocol is active, the Avanstar family control program will assert the RTS line until the Input Buffer High Water Mark is reached. At that time the RTS line will be negated. The RTS line will be asserted once again only after the number of characters in the input buffer falls below the Input Buffer Low Water Mark. This protocol is implemented in the Avanstar family control program. The blocking status is updated when this protocol is used.

Bit 7 Enable Modem Control/Status

Setting this bit makes the following functions available through the dual port:

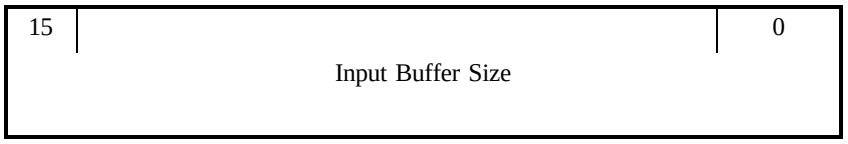
- Direct control of the DTR and RTS handshake lines.
- Ability to send Break streams.
- Ability to read the status of the CTS, DSR, RI, and DCD handshake lines.

These capabilities are provided through the use of the Modem Control and the Modem Status fields of the CCB.

Bit 13 Interface Type

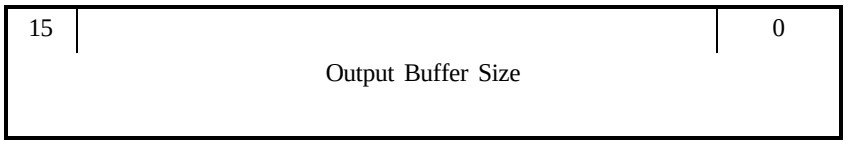
The device driver communicates with the control program through this bit in order to select the interface type. A "1" in this bit selects EIA-422; a "0" selects EIA-232. After this bit has been set or cleared, bit 0 or bit 1 of the appropriate Channel Command field must be set in order to change the interface type.

Input Buffer Size (R/W) CCB Offset: 0006H



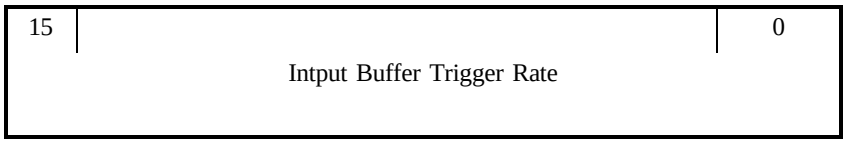
This field determines the number of bytes of the dual port RAM allocated for receiving characters. A minimum value of 0002H is required to use a channel; the upper bound is limited only by the amount of dual port RAM available. The value of this field should not be changed while any channel is transmitting or receiving data because characters will be lost.

Output Buffer Size (R/W) CCB Offset: 0008H



This field determines the number of bytes of the dual port RAM allocated for transmitting characters. A minimum value of 0002H is required to use a channel; the upper bound is limited only by the amount of dual port RAM available. The value of this field should not be changed while any channel is transmitting or receiving data because characters will be lost.

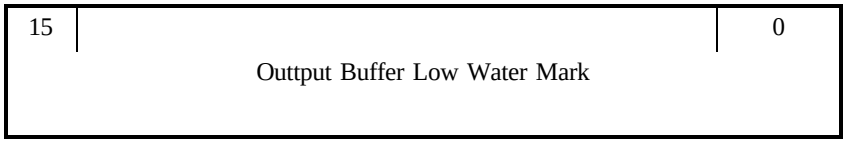
Input Buffer Trigger Rate (R/W) CCB Offset: 000AH



This field defines the number of characters that must be received before the host PC is alerted to a service request. A service request will also be indicated if any characters were received and the most recent character was received more than four character times in the past. The maximum value is 32767.

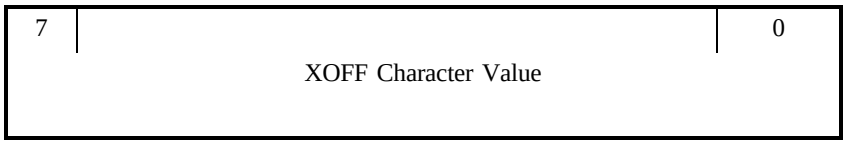
If interrupts from the Avanstar family board are disabled, the Input Buffer Service Request word of the GCB will still be updated. A value of 0 will indicate a service request on each character received.

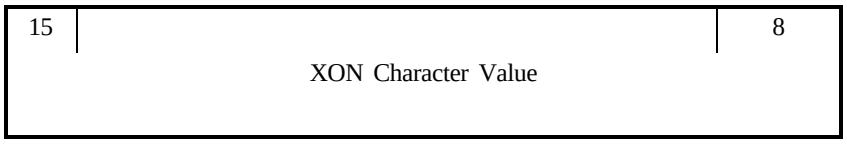
Output Buffer Low Water Mark (R/W) CCB Offset: 000CH



This field defines the number of characters that must be left in the output buffer for the host PC to be alerted to a service request. If interrupts from the Avanstar family are disabled, the Output Buffer Service Request field of the GCB will still be updated.

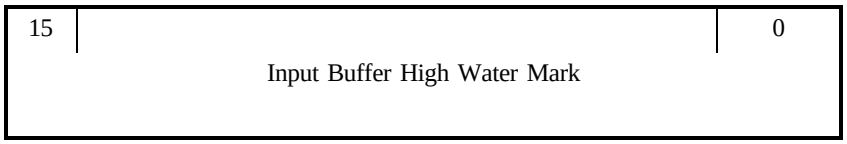
IXON Characters (R/W) CCB Offset: 000EH





When IXON is enabled in the Line Protocol field, the IXON Characters field determines the characters that, when received, start or stop output. These values are used in conjunction with the IXON and IXANY protocols described earlier in the Line Protocol field description. If both bytes are zero, the default XON (11H) and XOFF (13H) values are used.

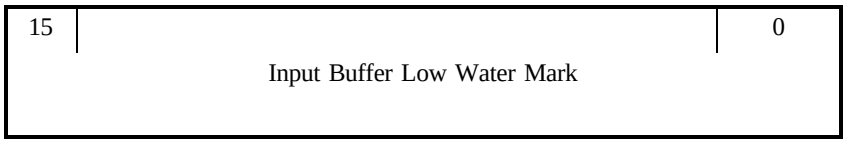
Input Buffer High Water Mark (R/W) CCB Offset: 0010H



This field defines the number of characters that need to be in the input buffer for an XOFF to be transmitted (IXOFF line protocol) or for RTS to be negated (Input Buffer Controls RTS line protocol). This value must be less than the Input Buffer Size.

If both the Input Buffer High Water Mark and Low Water Mark are zero, this value defaults to 32 characters less than the Input Buffer Size.

Input Buffer Low Water Mark (R/W) CCB Offset: 0012H

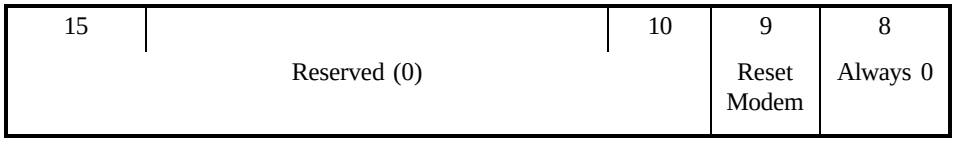


This field defines the number of characters that need to be left in the input buffer for an XON to be transmitted (IXOFF line protocol) or for RTS to be asserted (Input Buffer Controls RTS line protocol). This value must be less than the Input Buffer High Water Mark value.

If both the Input Buffer High Water Mark and Low Water Mark are zero, this value defaults to 64 characters less than the Input Buffer Size.

Channel Command (R/W) CCB Offset: 0014H

7	6	5	4	3	2	1	0
Disable Transmitter	Enable Transmitter	Disable Receiver	Enable Receiver	Flush Output Buffer	Flush Input Buffer	Configure Channel (not UART)	Configure Channel and UART



Setting one or multiple bits in this field to "1" sends the specified commands to the Avanstar family control program. The Avanstar family control program will then perform the commands specified on the channel, write a status value into the Channel Status field, and write a 0000H into the Channel Command field.

Bit 0 Configure Channel and UART

Setting this bit causes these parameters to be configured:

- Baud Rate
- Data Format
- Line Protocol
- Input Buffer Size
- Output Buffer Size
- IXON Characters
- Output Buffer Low Water Mark
- Input Buffer Trigger Rate
- Input Buffer High Water Mark
- Input Buffer Low Water Mark
- Modem Control
- IXOFF Characters
- Interface Type

This command does not reset the input and output buffer pointers unless either buffer size changes. In this case, both pointers on every channel are reset. The Modem Control field is read, and the Modem Control Lines are set accordingly when this command is issued.

Bit 1 Configure Channel (Not UART)

Setting this bit causes these parameters to be configured:

- Input Buffer Size
- Output Buffer Size
- IXON Characters
- Output Buffer Low Water Mark
- Input Buffer Trigger Rate
- Input Buffer High Water Mark
- Input Buffer Low Water Mark
- Modem Control
- IXOFF Characters
- Interface Type

This command does not reset the input and output buffer pointers unless either buffer size changes. In this case, both pointers on every channel are reset.

The Modem Control field is read, and the Modem Control Lines are set accordingly when this command is issued.

Bit 2 Flush Input Buffer

Setting this bit causes both input buffer pointers to be set to the Input Buffer Starting Address.

Bit 3 Flush Output Buffer

Setting this bit causes both output buffer pointers to be set to the Output Buffer Starting Address.

Bit 4 Enable Receiver

Setting this bit causes this channel's receiver to be enabled. This allows it to receive characters.

Bit 5 Disable Receiver

Setting this bit causes this channel's receiver to be disabled. This inhibits it from receiving any characters.

Bit 6 Enable Transmitter

Setting this bit causes this channel's transmitter to be enabled. This allows it to send characters.

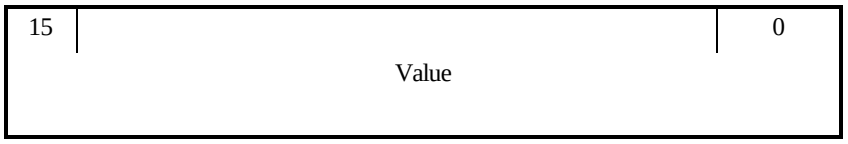
Bit 7 Disable Transmitter

Setting this bit causes this channel's transmitter to be disabled. This inhibits it from sending any characters.

Bit 9 Reset Modem

If a modem panel is attached, setting this bit causes the channel's modem to execute a hardware reset.

Channel Status (R/W) CCB Offset: 0016H



This field reports the status of the last command which was executed by setting bits in the Channel Command field.

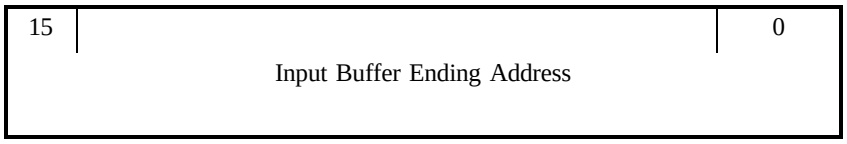
Possible values are:

Value	Definition
0000H	No Error
0001H	Invalid Baud Rate
0002H	Invalid Data Format
0003H	Invalid Line Protocol
0004H	Invalid Input Buffer Size
0005H	Invalid Output Buffer Size
0006H	Invalid Input Buffer Trigger Rate
0007H	Invalid Output Buffer Low Water Mark
0008H	Invalid XON/XOFF Characters
0009H	Invalid Input Buffer High Water Mark
000AH	Invalid Input Buffer Low Water Mark
000BH	Non-functional UART

Input Buffer Starting Address (RO) CCB Offset: 0018H

This field contains the address of the start of the input buffer. This address is relative to the base of the dual port.

Input Buffer Ending Address (RO) CCB Offset: 001AH

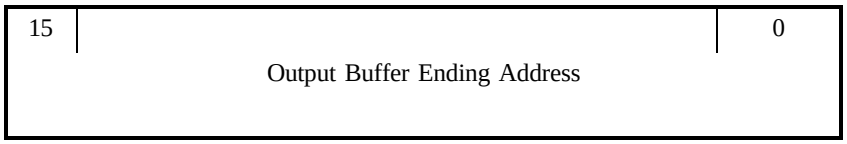


This field contains the address of the end of the input buffer. This address is relative to the base of the dual port.

Output Buffer Starting Address (RO) CCB Offset: 001CH

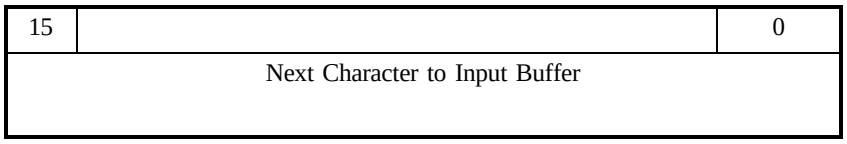
This field contains the address of the start of the output buffer. This address is relative to the base of the dual port.

Output Buffer Ending Address (RO) CCB Offset: 001Eh



This field contains the address of the end of the output buffer. This address is relative to the base of the dual port.

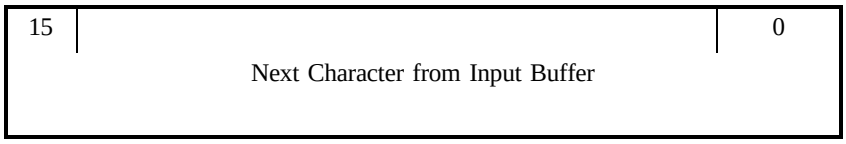
Next Character to Input Buffer (RO) CCB Offset: 0020H



This field contains the address of the next available space in the input buffer. This address is relative to the base address of the dual port. Each time the Avanstar family adapter receives a character, it is placed at this location, and this pointer is incremented by one.

The input buffer is a circular buffer. When the pointer reaches the end of the buffer, the next character will be wrapped around to the start. The Avanstar family control program performs this task automatically.

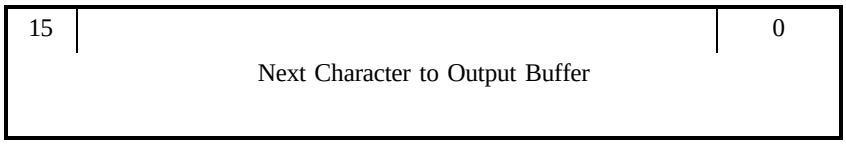
Next Character from Input Buffer (R/W) CCB Offset: 0022H



This field contains the address of the next character to be read from the input buffer. This address is relative to the base address of the dual port. The host interface program must increment this pointer after reading the character in the input buffer. When this pointer reaches the end of the input buffer, it must be wrapped around to the start by the host interface program.

This pointer should always be logically at or behind the Next Character to Input Buffer. When the two pointers are equal, there are no characters in the input buffer.

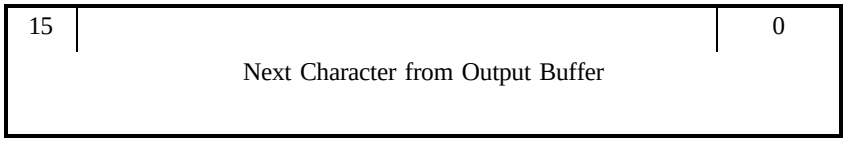
Next Character to Output Buffer (R/W) CCB Offset: 0024H



This field contains the address of the next available space in the output buffer. This address is relative to the base address of the dual port. The host interface program must increment this pointer after placing a character in the output buffer.

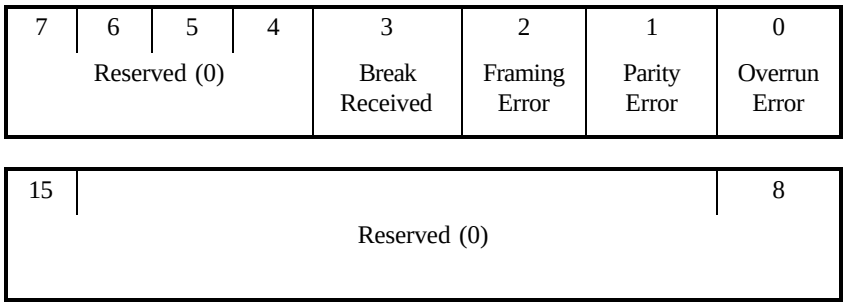
This pointer should always be logically at or ahead of the Next Character from Output Buffer. When the two pointers are equal, there are no characters in the output buffer. When the Next Character to Output Buffer pointer reaches the end of the Output Buffer, it must be wrapped around to the start by the host interface program. The host interface program must make sure that this pointer does not wrap around and overtake the Next Character from Output Buffer pointer because this will cause characters to be lost.

Next Character from Output Buffer (RO) CCB Offset: 0026H



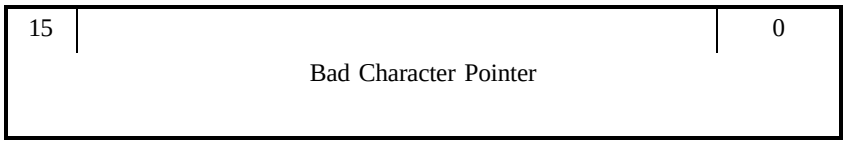
This field contains the address of the next character to be read from the output buffer. This address is relative to the base of the dual port. The Avanstar family control program increments this pointer after reading the character from the output buffer. Also, the Avanstar family control program will wrap the pointer around to the start when it reaches the end of the output buffer.

Communication Error Status (X) CCB Offset: 0028H



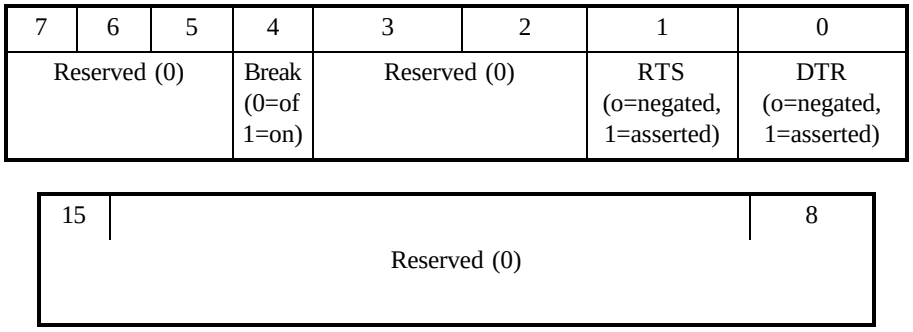
This field contains a bit pattern of all of the communication errors which have occurred since the last time the application cleared it.

Bad Character Pointer (R/W) CCB Offset: 002AH



This field contains the address of the first occurrence of an error in the input buffer. This address is relative to the base address of the dual port. After reading this field, the host interface program should reset it to zero. The Avanstar family control program will not update this field unless it has been cleared to zero.

Modem Control (R/W) CCB Offset: 002CH



When the Modem Control/Status bit of the Line Protocol field is set, the Avanstar family control program continually monitors the Modem Control field. Any change to this field will be immediately acted upon. This field is also read and used when a Configure Channel command (Bit 0 or 1 of the Channel Command field) is executed.

The break bit is a one-shot bit. Setting this bit causes a break of a fixed length to be sent. The control program clears this bit after initiating the break.

Modem Status (RO) CCB Offset: 002EH

7	6	5	4	3	2	1	0
Reserved (0)				DCD (o=negated, 1=asserted)	RI (o=negate 1=asserted	DSR (o=negated, 1=asserted)	CTS (o=negated, 1=asserted)

15							8
Reserved (0)							

When the Modem Control/Status bit of the Line Protocol field is enabled, this field is continuously updated by the Avanstar family control program. Any change to the modem status lines will be immediately acted on. This field is also updated when a Configure Channel command (bit 0 or 1 of the Channel Command field) is executed.

Blocking Status (RO) CCB Offset: 0030H

7	6	5	4	3	2	1	0
Reserved (0)		RTS is Negated	Transmitted an XOFF	Transmitter is Blocked by CTS Negated	Transmitter is Blocked by an XOFF	Transmitter is Disabled	Receiver is Disabled

15							8
Reserved (0)							

This field reflects the current blocking state of the channel.

NOTE:

Bit 3 is updated only when the Modem Control/Status bit of the Line Protocol field is enabled. Bit 5 is updated only when the Input Buffer Controls RTS bit of the Line Protocol field is enabled.

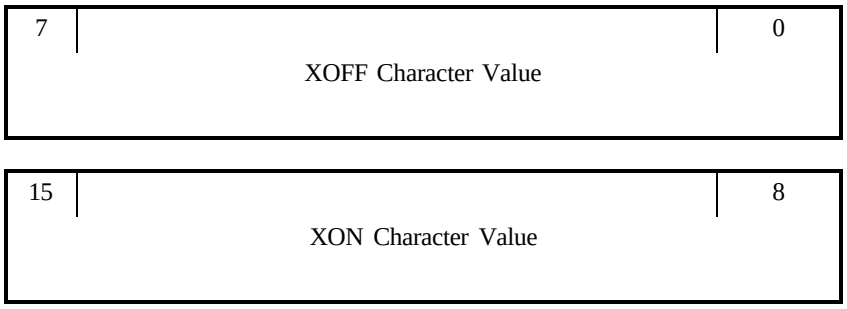
Character Received Flag (R/W) CCB Offset: 0032H

15							0
Character Received Flag							

This field is set to FFFFH on every character that is received on this channel. This field can be used by the host interface program to check if characters have been received. To ensure that the flag reflects the correct state, the host interface program should use the following procedure to access and update the flag.

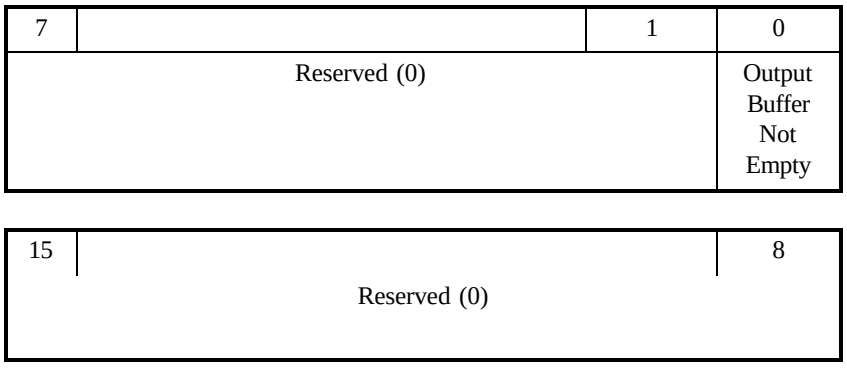
1. Read the Character Received Flag field. If the flag is zero, no characters are available, and you should exit this procedure.
2. Read all the characters that are available and update the Next Character from Input Buffer field following the procedure given in section 4.5.2.
3. Clear the Character Received Flag field.
4. Check if the Next Character from Input Buffer field and Next Character to Input Buffer field are equal. If these fields are equal, no characters are available, and you should exit this procedure. If the fields are not equal, more characters are available, and you should go to Step #2.

IXOFF Characters (R/W) CCB Offset: 0034H



When IXOFF is enabled in the Line Protocol field, the IXOFF Characters field selects the characters that are transmitted to start or stop the remote transmitter. As described in the Line Protocol field description, these values are used in conjunction with the IXOFF protocol. If both bytes are zero, the default XON (11H) and XOFF (13H) values are used.

Channel Status 2 (RO) CCB Offset: 0036H



This field reflects the current status of the channel.

Bit 0 Output Buffer Not Empty

This bit is set to 1 when the Output Buffer is not empty (contains characters) or when the UART is in the process of transmitting characters (transmitter is not empty). This bit is cleared to 0 only when the Output Buffer is empty and the UART is not transmitting characters.

Buffer Area

The input and output buffers for the channels are used to transfer characters from the Avanstar family board to the host and to transfer characters from the host to the Avanstar family board.

Transmitting Characters

To transmit a character to a channel, the character must be written to the output buffer of the appropriate channel. Do this by using the Next Character to Output Buffer value as a pointer to identify the next empty location in the output buffer. Place the character into that location and increment the Next Character to Output Buffer by one.

After the pointer has been incremented to the upper bound of the output buffer, it must be wrapped around to the beginning. This is necessary because the output buffer is circular.

To do this, compare the pointer with the Output Buffer Ending Address value. If the Next Character to Output Buffer value is greater than the Output Buffer Ending Address, set the pointer equal to the Output Buffer Starting Address.

The Avanstar family control program uses the Next Character from Output Buffer pointer to keep track of transmitted characters. In situations where large amounts of data are being transmitted, the Next Character to Output Buffer pointer may possibly overtake the Next Character from Output Buffer pointer.

This may occur because characters can be transferred to memory much faster than they can be transmitted from the UART. The host interface program must check that the Next Character to Output Buffer pointer does not overrun the Next Character from Output Buffer pointer. Otherwise, characters will be lost.

Receiving Characters

Characters are available when the values of the Next Character from Input Buffer and of the Next Character to Input Buffer are not equal. Once this condition is detected, characters may be retrieved using the procedure described below.

To read a character, use the Next Character from Input Buffer value as a pointer. This word is a pointer to the next available character.

After reading the character, increment the Next Character from Input Buffer pointer by one to point to the next character. This process is necessary because the Avanstar family control program uses the offset value to ensure that characters which have not been read are not overwritten by newly received characters.

After the pointer has been incremented to the upper bound of the input buffer, it must be wrapped around to the beginning. This is necessary because the input buffer is a circular buffer.

To do this, compare the pointer with the Input Buffer Ending Address value. If the Next Character from Input Buffer value is greater than the Input Buffer Ending Address value, set the pointer equal to the Input Buffer Starting Address value.

This procedure of reading and updating the pointer may continue until the Next Character from Input Buffer value equals the Next Character to Input Buffer value. This will occur only when the input buffer is empty.

Communication Errors

When the Avanstar family control program detects that it has received an erroneous character, the following steps are taken.

1. If bit 8 of the Data Format field of the Channel Control Block is cleared to 0, the byte value FFH is placed in the dual port input buffer. If the bit is set to 1, the erroneous character is placed in the dual port input buffer.
2. If the Bad Character Pointer field is 0, the Avanstar family control program updates it with the input buffer address of the bad character.
3. The Avanstar family control program sets the appropriate bit in the Communication Error Status field.
4. The Communication Error Service Request field of the Global Control Block is updated.
5. The Global Service Request field of the GCB is updated.
6. The Next Character to Input Buffer pointer is updated.
7. If enabled, an interrupt is generated.

The procedure that the Host Interface Program should use to detect and handle communication errors is as follows:

1. Read characters as described in section 4.5.2.
2. If the Bad Character Pointer field and the Next Character from Input Buffer field are equal, then the character is bad.
3. Read the Communication Error Status field and clear it to 0.
4. Set the Bad Character Pointer field to 0.

There are some limitations with the current implementation of communication error-handling.

1. Error status is not available on individual characters since it is cumulative.
2. There is no way to determine if all FFH characters were actually received in error if there are multiple FFH characters in the input buffer.

Configuring Parameters

When the Avanstar family control program is downloaded, each channel is initialized to the default configuration parameters. These parameters may be changed in the following way.

1. Write the new configuration parameters into the appropriate Channel Control Block.
2. Set the Channel Command field for the desired configuration type.
3. Wait for the Channel Command field to return to 0000H. After the Channel Command field returns to 0000H, check the Channel Status word for any errors. If an error has occurred, the Channel Status field will contain the error code.

Service Requests

Service Requests are important conditions that the Avanstar family control program detects and notifies the host PC about. When the Avanstar family control program detects that one of the service request conditions has occurred, the following steps are taken:

1. The condition causing the service request is completely handled by the Avanstar family control program, including updating pointer and status fields.
2. The corresponding Service Request field in the GCB is updated.
3. The Global Service Request field is updated.
4. If enabled, an interrupt is generated.

The Service Request fields need to be updated by both the Avanstar family processor and the host PC. This may potentially cause a service request bit to be lost. To avoid this problem, the host PC must access and clear the field using the XCHG instruction with the Register Operand cleared to zero. An example segment of code is given below:

```
mov     ax, 0D0000H         ;assume dual port seg = D000H
mov     es, ax              ;es points to dual port seg
sub     ax, ax              ;zero out ax
xchg    ax, es:[GlobSR]     ;get global service bits in ax
                            ;and zero out global service bits
```

It is possible that a service request bit could be set without the condition actually existing. Before handling the service requests indicated by the Service Request fields, always check the pointer and status fields of the channel.

Interrupt Handling

It is possible to have the Avanstar family control program interrupt the host PC when a service request condition occurs. Interrupts are enabled by setting the Interrupt Acknowledge Bit in the Global Command Word 2 field of the Global Control Block. If the Avanstar family control program had made any service requests prior to setting this bit, an interrupt will be generated when it is set.

The Avanstar family control program allows multiple Avanstar family boards to share the same IRQ line. The Interrupt Acknowledge Bit in Global Command Word 2 must be set on all Avanstar family boards sharing an IRQ line before any of them will be able to generate an interrupt.

It is possible that extra interrupts might be generated by the Avanstar family control program. Make sure your interrupt handler can handle this condition.

The following is pseudo code for a typical interrupt handler:

```
PROC IntHandler
   Enable interrupts;
   Save registers on stack;

FOR each Avanstar family board sharing interrupt
   /* Avanstar 100m only */
   Read from offset 3FF8 in dual port
   /* re-enable Avanstar family control program interrupts */
   Set Interrupt Acknowledge Bit in Global Command 2;
   /* check service requests & service them */

IF Global Service Request != 0 THEN
   Global Service Request := 0;
   Use the XCHG instruction as described in section 4.5.5 to access
and clear all service request      fields;
   Service all the requests that were indicated;

   ENDIF

END FOR
   /* interrupt handler completion & exit */
   Send non-specific EOI to interrupt controller;
   Restore registers from stack;
   Return from interrupt;

END PROC
```

Chapter 5: Reset and Download Procedure

Avanstar Reset And Download Procedures

Because an Avanstar family board has no onboard ROM, a control program must be downloaded to it before use. This section contains information and a pseudocode procedure for downloading a program to an Avanstar family board and starting its execution.

At power-on, the board is in the download mode which holds the 80186 in the reset state and overlays the local RAM onto the dual port memory space. Setting the DOWNLOAD bit of a board I/O register brings up the 80186 and resets host access to dual port memory. Each member of the Avanstar family is addressed a little differently, but the basic download procedure remains the same. The ISA board has several directly-addressable I/O registers.

ISA Board Procedures

To reset the Avanstar ISA board, the Download bit in Control Register 1 must be cleared to 0. This bit holds the board's processor in the reset state. The Download bit must remain cleared for at least 1 millisecond in order for the board to be properly reset. It may then be set to 1.

CAUTION

Be sure to preserve the state of all unused bits when configuring I/O Registers. Otherwise, the board may function improperly.

Prior to bringing the board out of reset for the first time, the control program is loaded into local memory. Conveniently, while the Download bit is reset, the local RAM is overlaid onto the dual port memory space. However, since the board contains 64K of local RAM and only 16K of dual port memory, a windowing scheme is required to access all of local RAM. Four MemoryBankSelect bits provided in Control Register 2 are used to select one of four (16 in the case of an Avanstar 200i board) 16K blocks of local RAM which will be currently addressed in the dual port memory space.

The following steps should be taken to download a control program:

1. Put the board in download mode by clearing the Download bit in Control Register 1 to 0.
2. Enable memory accesses to the board by setting the MemoryEnable bit in Control Register 2 to 1.
3. Select the block of local RAM to overlay the dual port memory space by writing the appropriate value to the MemoryBankSelect bits in Control Register 2.
4. Write the proper block of control program data to the local RAM which now overlays the dual port RAM.

NOTE

The standard control program file provided by Industrial Computer Source is in Intel hex format. If you intend to download this file, you will need to convert it to a binary image before copying it into the local RAM.

Repeat the preceding steps (except #1) to download to all blocks of local RAM, if necessary.

Once the control program has been loaded (including the reset vector at FFFF0), the board needs to be placed into the normal operating mode to start the 80186 and to map the dual port RAM to the host system's memory space. Put the board in normal operating mode by setting the Download bit in Control Register 1 to 1.

The following is pseudo-C code for downloading a control program to all boards in an ISA system:

```
 /*Download to all Avanstar ISA boards in the system.  */
BYTE iobase;
BYTE iobases[8] = {0x200, 0x208, 0x300, 0x308, 0x600, 0x608,
0x700, 0x708};
void loada100i(void)
{
   BYTE bank;
   WORD id;
   ULONG dpaddr;
/* Check all valid I/O addresses */
for (iobase=0; iobase<7; iobase++)
{
   /* See if register contains ID 0xEC13 or 0x13EC*/
   id = (inp(iobase+BOARDIDREG) << 8) + inp(iobase+BOARDIDREG);
   if ((id == 0xEC13) || (id == 0x13EC))
   {
/* Set download mode */
outp(iobase+CONTROLREG1, inp(iobase+CONTROLREG1) & 0xFD);
/* Get the dual port address */
dpaddr = (((ULONG)(inp(iobase+DPADDREG))) << 12) & 0x000FC000;
/* Clear entire local RAM */
for (bank=0; bank<3; bank++) {/* Use "bank<15" for A200*/
selectbank(bank);    /* Select local RAM bank */
FILL 16K BANK WITH 00H;
}
```

```
COPY DATA INTO THE BOARD'S LOCAL RAM (SELECT BANK AS NEEDED);
/*  Set  normal  operating  mode*/  outp(iobase+CONTROLREG1,
inp(iobase+CONTROLREG1) | 0x02);
/* Wait for control program to report that it's ready*/
do {
   if (inp(iobase+CONTROLREG1) & 0x01 == 1)
   break;
} FOR 10 SECONDS;
if (inp(iobase+CONTROLREG1) & 0x01 == 0)
   printf("Board not ready at iobase %x", iobase);
else
   printf("Download successful to board at iobase %x", iobase);
        }
   }
}
/* Select new local RAM bank */
void selectbank(BYTE bank)
{
   BYTE temp;
   temp = inp(iobase+CONTROLREG2) & 0FCH;
   /* Get CR2 (save extra bits) */
   outp(iobase+CONTROLREG2, temp | bank);
   /* Set new bank select bits*/
}
```

EISA Procedures

The EISA Specification describes a standard set of adapter registers which are encoded with the adapter slot number. For example, the first board ID register is located at I/O address xC80H, where x = 1 to 8 (the slot number).

To reset the EISA board, the IOCHKRST bit in the Board Control Register (xC84H) must be set to 1. This bit holds the board's processor in the reset state. This bit must remain set for at least 500 nanoseconds in order for the board to be properly reset. It may then be reset to 0. Setting this bit resets and disables the board by clearing the ENABLE bit. So, after pulsing the IOCHKRST bit, the ENABLE bit must be set to 1.

CAUTION

Be sure to preserve the state of all unused bits when configuring EISA Registers. Otherwise, the board may function improperly.

Prior to bringing the board out of reset for the first time, the control program is loaded into local memory. Conveniently, during Download Mode (defined as the state of the board just prior to step 8 below), the local RAM is overlaid onto the dual port memory space. However, since the board contains 64K of local RAM and only 32K of dual port memory, a windowing scheme is required to access all of local RAM. The Local RAM Bank Select bit in the Download Register is used to select one of the two 32K blocks of local RAM which will be currently addressed in the dual port memory space.

The following steps should be taken to download a control program:

1. Disable access to the dual port memory space by resetting the Dual Port Enable bit of the Dual Port Enable Register (xCAEH) to 0.
2. Reset the board by setting the IOCHKRST bit in the Board Control Register (xC84H) to 1.
3. Setup the EISA interface for local RAM access by writing 4EH to the Dual Port Mode Register (xCA1H).
4. Enable the EISA interface by setting the ENABLE bit of the Board Control Register (xC84) to 1. Do this twice.
5. Map the board's local RAM to the dual port memory space by resetting the DOWNLOAD bit of the Download Register (xCADH) to 0.
6. Select the lower half of local RAM to map to the dual port memory space by resetting the Local RAM Bank Select bit of the Download Register (xCADH) to 0.
7. Enable access to the dual port memory space by setting the Dual Port Enable bit of the Dual Port Enable Register (xCAEH) to 1.
8. Write the proper block of control program data to the local RAM which now overlays the dual port RAM.

NOTE

The standard control program file provided by Industrial Computer Source is in Intel hex format. If you intend to download this file, you will need to convert it to a binary image before copying it into the local RAM.

Repeat steps 6 and 8 to download to all blocks of local RAM, if necessary.

Once the control program has been loaded, including the reset vector at FFFF0, the board needs to be placed into the normal operating mode to start the 80186 and to map the dual port RAM to the host system's memory space. Execute the following steps:

1. Disable access to the dual port memory space by resetting the Dual Port Enable bit of the Dual Port Enable Register (xCAEH) to 0.
2. Map the board's dual port RAM to the dual port memory space by setting the DOWNLOAD bit of the Download Register (xCADH) to 1.

3. Setup the EISA interface for dual port RAM access by writing 6EH to the Dual Port Mode Register (xCA1H).
4. Enable access to the dual port memory space by setting the Dual Port Enable bit of the Dual Port Enable Register (xCAEH) to 1.

The following is pseudo-C code for downloading a control program to all boards in an EISA system:

```
/*Download to all Avanstar EISA boards in the system.*/
BYTE slot;
#define in_eisa(reg)  inp((slot << 12) + reg)
#define out_eisa(reg,val)  outp((slot << 12) + reg, val)
void loada100e(void)
{
   BYTE block;
   ULONG dpaddr;

   /* Check all EISA slots */
   for (slot=0; slot<7; slot++)
   {
        /* See if ID registers contain ID 0x4CF4 - 01 */
        if ( (in_eisa(IDREG0) == 0x4C) &&
             (in_eisa(IDREG1) == 0xF4) &&
             (in_eisa(IDREG2) == 0x01) )
        {
             /* Get the dual port address */
             dpaddr = (((ULONG)in_eisa(MACR0) << 8) |
             ((ULONG)in_disa(MACR1) << 16)) & 0x000F8000;

             /* Reset the board */
out_eisa(DPENREG, 0);/* Disable access to dual port mem space */
out_eisa(BDCTRLREG, 0x04);/* Reset & disable the board */
out_eisa(DPMODEREG, 0x4E);/* Setup forlocal RAM access */
out_eisa(BDCTRLREG,0x01); /* Enable the board */
out_eisa(BDCTRLREG, 0x01); /* Enable the board - twice */
out_eisa(DOWNLOADREG, 0x00);  /* Set download mode, block 0 */
out_eisa(DPENREG,0x10);/*Enable access to dual port mem space*/
/* Clear entire local RAM */
for (block=0; block<2; block++)
{
```

```
selectblock(block);/* Select local RAM block */
   FILL 32K BLOCK WITH 00H;
}
COPY DATA INTO THE BOARD'S LOCAL RAM (SELECT BLOCK AS NEEDED);


/* Set normal operating mode */
out_eisa(DPENREG,0);/* Disable access to dual port mem space */
out_eisa(DOWNLOADREG,0x01);/* Set normal operating mode */
out_eisa(DPMODEREG,0x6E);/* Setup for dual port RAM access */
out_eisa(DPENREG,0x10);  /*Enable access to dual port mem space */
/* Wait for control program to report that it's ready */
do {
   if ((in_eisa(BDSTATREG) & 0x01) == 1) break;
} FOR 10 SECONDS;
if ((in_eisa(BDSTATREG) & 0x01) != 1)
   printf("Board not ready in slot %d", slot); else
   printf("Download successful to board in slot %d", slot);
        }
   }
}
/* Select new local RAM block */
void selectblock(BYTE block)
{
   out_eisa(DOWNLOADREG, slot << 1);/* Set new bank select bit */
}
```

Chapter 6: MicroProcessor Hardware Interface

Introduction

This chapter contains information on the hardware that can be accessed by the Avanstar family microprocessor. You will need this information if you are writing control program software for an Avanstar family board.

Processor Memory

The Avanstar family board main processor memory is 64K bytes of static RAM. This memory is accessed by the host processor when in Download Mode and by the board processor when in Normal Mode. Since there is no ROM, the control program must be downloaded to this memory area before the processor is enabled.

Immediately after the processor comes out of reset executing code at the reset vector (FFFF0H), the Lower Chip Select (LCS) should be enabled to allow access to the lower memory range of 00000H - 0FFFFH. This is done by programming the LMCS register of the processor for 64K memory size, 0 wait states and internal ready operation. For further information on the 80186 processor, refer to the Intel iAPX 86/88, 186/188 Programmer's Reference.

Dual-Ported Memory

The Avanstar 100 family boards have 16K bytes (32K bytes - EISA only) of dual-ported memory. The Avanstar 200i has 256K bytes of dual-ported memory. This memory, which can be accessed by both the board processor and the host processor, is enabled by the board processor's MCS0 line. In order for the board to access the dual-ported memory correctly, the MMCS register of the 80186 processor must be programmed for 0 wait state/external ready operation. The address bits of the MPCS and MMCS registers should be programmed as follows:

	ISA bus boards		EISA bus boards
Dual-Port Size	16K	256K	32K
MPCS Total Block Size	256K	128K	64K
MMCS Base Address	80000H	40000H	40000H

The starting dual-ported memory address is the same as the MMCS Base Address.

UART Addressing

The UARTs can be accessed only by the board processor, not by the host PC. The UARTs are memory-mapped and use the processor's MCS1 line. For example, the first UART on each ISA, EISA and Micro Channel board is addressed at 90000H, 48000H and 44000H, respectively.

Each Avanstar family external connection panel uses either two or four 4-port CD1400 UARTs. The UARTs and communication ports are mapped as follows:

Port Assignments Base

UART	16-Port8-Port	Modem Panel	Address
1	0,1,8,9 0,1,-,-	0,1,2,3	MCS1
2	2,3,10,11	2,3,-,- 4,5,6,7	MCS1+100H
3	4,5,12,13	4,5,-,- -,-,-,-	MCS1+200H
4	6,7,14,15	6,7,-,- -,-,-,-	MCS1+300H

where a dash indicates that that UART channel is unused.

Since all access to the UARTs is byte-wide (D0-D7), all operations must be performed on even (word) address boundaries. This implies that register addresses within each UART must be doubled. For example, although the GFRCR UART register is defined as being at offset of 40H from the base of the UART, it is accessed at an offset of 80H.

Refer to the Cirrus Logic CL-CD1400 data sheet for UART register descriptions.

Board I/O Registers

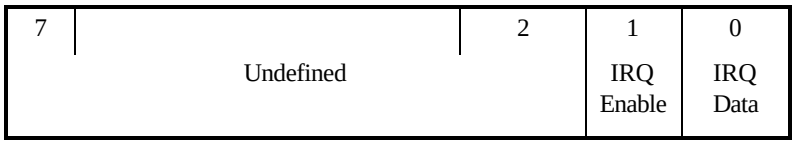
There are two I/O-mapped registers on each Avanstar family board which are used to communicate with the host processor. One register is written by the board processor to indicate a ready/not ready status of the control program, and the other is used to generate an interrupt to the host PC.

ISA Registers

Signal Register (WO) I/O Address: 400H

Writing to this decoded I/O address sets the Program Ready Bit of the host-referenced Control Register 1 to indicate that the control program has completed initialization. This bit is automatically cleared on download.

Interrupt Register (WO) I/O Address: 480H



Bit 0 IRQ Data

Toggling this bit from 1 to 0 to 1 causes an interrupt to the host PC. This bit is automatically set on download.

Bit 1 IRQ Enable

Clearing this bit enables interrupts from the board to the host PC. This bit is automatically set on download.

A practical way to generate an interrupt to the host PC would be to write a 00H to the Interrupt Register, followed by a 03H. This interrupt is latched on the host PC.

EISA Registers

Signal Register (WO) I/O Address 400H

Writing to this decoded I/O address sets the Board Ready Bit of the host-referenced Board Status Register to indicate that the control program has completed initialization. This bit is automatically cleared on reset or download.

Interrupt Register (WO) I/O Address 480H

Writing to this decoded I/O address will post an interrupt to the host PC. This interrupt is latched on the host PC.

UART Interrupts

The Cirrus Logic CL-CD1400 UARTs supply three interrupts to the 80186 processor. INT0 is used as a receiver interrupt, INT1 is used as a transmitter interrupt, and INT2 is used as a modem interrupt. The Avanstar family board also has three timers integrated into its microprocessor which can be configured to interrupt the CPU. Please refer to the Intel iAPX 86/88, 186/188 Programmer's Reference for more information.

In order to service these interrupts properly, the processor must return an acknowledge signal to the UARTs. The Avanstar family board provides three I/O mapped locations which, when read, supply the needed acknowledge to the UARTs. In addition, reading the acknowledge locations returns interrupt status information as described in the CD1400 data sheet.

The interrupt acknowledge locations are accessed via the processor's PCS4 line. The processor's MPCS register must be programmed to use "external ready" for proper operation of the acknowledge hardware.

The interrupt acknowledge registers are addressed as follows:

Receive Acknowledge	PCS4+0
Transmit Acknowledge	PCS4+2
Modem Acknowledge	PCS4+4

Control Program Development

When developing a control program for the Avanstar family board, keep these details in mind:

The board uses the Intel 80186 microprocessor. This processor resets to FFFF0. Your downloaded control program should have startup code at this location.

The 80186 microprocessor requires that the Chip Select Unit be initialized.

Downloaded software is stored in the local RAM of the Avanstar family board. It is best to start your program at 00400H. This leaves the interrupt vector table empty.

Your code is completely responsible for all initialization of the 80186 microprocessor and all peripheral devices. This includes (but is not restricted to) the following:

- Initializing the stack by setting the stack segment (SS) and the stack pointer (SP).
- Initializing the Chip Select Unit.
- Initializing the Peripheral Chip Select lines.
- Initializing any interrupt vectors which may be used.
- Initializing on-chip peripheral devices (i.e., timers, dma, etc.).

While the ability to download programs allows you to use standard DOS program development tools to develop control programs for the Avanstar family adapters, consider these subtle differences:

- There is no DOS, BIOS, or any other operating system execution on the adapter. Do not make any DOS or BIOS calls using INT instructions because these vectors are not initialized.
- Do not attempt to return to DOS if the control program completes execution or detects errors.
- The standard high level language (C, BASIC, Pascal, etc.) run-time start-up cannot be linked into your program.

The download programs supplied by Industrial Computer Source require the control program be in Intel hex format or Tektronix extended Tekhex format.

BUG REPORT

While we have tried to assure this manual is error free, it is a fact of life that works of man have errors. We request you to detail any errors you find on this BUG REPORT and return it to us. We will correct the errors/problems and send you a new manual as soon as available. Please return to:

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