Model ACB4-AT
Product Manual

MANUAL NUMBER : 00750-111-6D

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FOREWARD

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Manual Errors, Omissions and Bugs: A "Bug Sheet" is included as the last page of this manual. Please use the "Bug Sheet" if you experience any problems with the manual that requires correction.

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August 1997

Chapter 1: Installation

The ACB4-AT can be installed in any of the PC expansion slots, excluding J8 on the "XT" and Portable. Remove the PC case, remove the blank metal slot cover, and insert the board. Replace the screw, replace the case, and installation is complete. Install the DB-25 bracket for the second port in the next slot if you are using both ports.

NOTE:

Be sure to set the address and jumper options before installation.

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Chapter 2: Address Selection

The ACB4-AT occupies 8 consecutive I/O locations. A dip-switch (SW1) is used to set the base address for these locations. Be careful when selecting the base address as some selections conflict with existing PC ports. The following table shows several examples that usually do not cause a conflict.

Address	Binary	Switch Position Settings						
	A9 A0	1	2	3	4	5	6	7
238-23F	1000111XXX	OFF	ON	ON	ON	OFF	OFF	OFF
280-288	1010000XXX	OFF	ON	OFF	ON	ON	ON	ON
2A0-2A8	1010100XXX	OFF	ON	OFF	ON	OFF	ON	ON
2E8-2EF	1011101XXX	OFF	ON	OFF	OFF	OFF	ON	OFF
300-308	1100000XXX	OFF	OFF	ON	ON	ON	ON	ON
328-32F	1100101XXX	OFF	OFF	ON	ON	OFF	ON	OFF
3E8-3EF	1111101XXX	OFF	OFF	OFF	OFF	OFF	ON	OFF

Figure 1: Address Selection

Typically COM1:=3F8; COM2:=2F8h; COM3:=3E8h; COM4:=2E8h.

The following illustration shows the correlation between the dip-switch setting and the address bits used to determine the base address. In the example below, the address 300 Hex through 307 Hex is selected. 300 Hex = 11 0000 0XXXX in binary representation.

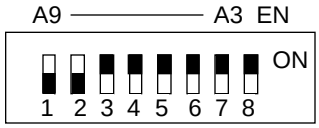


Figure 2: Switch Settings

Note that setting the switch “on” or “closed” corresponds to a “0” in the address, while leaving it “off” or “open” corresponds to a “1”.

Enable/Disable

The ACB4-AT can be enabled or disabled with switch position 8 on the dipswitch. The port is enabled with the switch “On” or “Closed” and disabled when “Off” or “Open”.

The relative I/O address of the ACB4-AT registers are as follows:

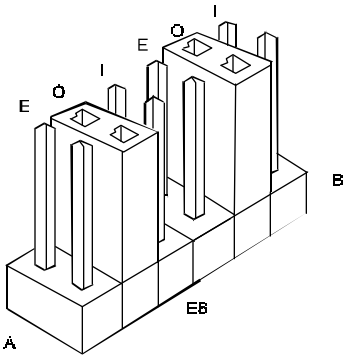
Base+0	Channel A Data Port
Base+1	Channel A Control Port
Base+2	Channel B Data Port
Base+3	Channel B Control Port
Base+4	Board Control/Status Port
Base+5	Reset TCIRQ

Where “Base” is the selected board base address.

Chapter 3: Option Selection

The ACB4-AT contains several jumper straps which must be set for proper operation. For jumper locations, refer to Figures 3 through 7.

E8: Sets the input/output clock modes for the transmit clock (TXC) and RS-485 driver enable. Please note that setting a jumper in position “I” and position “O” at the same time is not a valid option.



E	Channel.A RTS Enable (for RS-485 Mode only)
O	Transmit Clock Output Channel A
I	Transmit Clock Input Channel A
E	Channel B RTS Enable (for RS-485 Mode only)
O	Transmit Clock Output Channel B
I	Tansmit Clock Input Channel B

Figure 3: Header E8 Illustration. The default setting is jumpers in position "O"

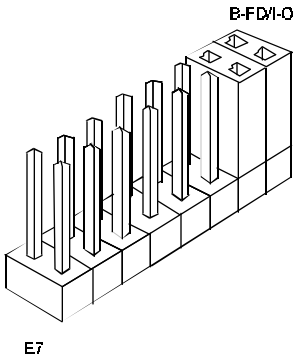
In addition to RS-530, the ACB4-AT is capable of RS-422 and RS-485 communications. E8 position “E” determines whether the RS-530 (and RS-485) transmit driver is enabled by the SCC (Serial Communications Controller) signal Request To Send (RTS) or always enabled. With the jumper installed, RTS enables the driver. Removing the jumper enables the driver regardless of RTS. This jumper should only be installed if you are running the board in a multidrop polled environment such as RS-485, and you have software that knows how to “talk” on the RS-485 bus.

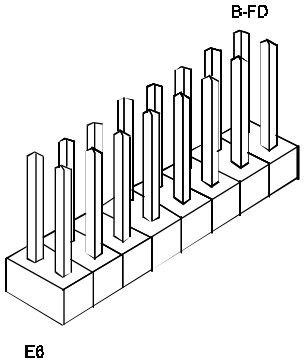
For normal point-to-point RS-530 and RS-422, remove the jumper.

E4-E7: E4-E7 select DMA (Direct Memory Access) mode of operation. Each channel of the SCC will function in half duplex or full duplex DMA modes. Full duplex means that DMA can be used for simultaneous transmit and receive. Half duplex DMA means that you can either transmit, or receive with DMA, but not simultaneously. The 8530 has two signals that correspond to DMA request signals, WAIT/REQ and DTR/REQ. E5 & E7 correspond to WAIT/REQ and E4 & E6 correspond to DTR/REQ. WAIT/REQ and DTR/REQ can be programmed to serve as DMA request lines (DRQ) by setting the appropriate bits in Write Register 1 and Writer Register 14 in the 8530. WAIT/REQ (E5 & E7) can be programmed for Transmit or Receive DMA transfers and DTR/REQ (E4 & E6) can be programmed for Transmit only. For additional information on the programming of the 8530 please refer to the Zilog 8530 Technical Manual. Please note that each DMA channel is selected by two jumpers. Only one DMA channel may be selected for each header block.

NOTE:

If DMA is not used, remove all of the jumpers on E4-E7 and install a jumper in position “N” of E2





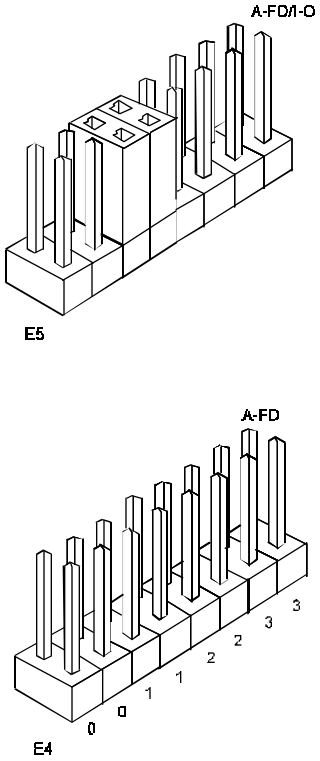


Figure 4: DMA Selection jumpers (shown in factory default settings)

E4 and E5 select the DMA Channel for Channel A of the SCC.

E6 and E7 select the DMA Channel for Channel B of the SCC.

NOTE:

DMA Channel 0 is not available on "XT" class machines, and DMA Channel 2 can only be used if the floppy disk DMA drivers are turned off. Please refer to the toolkit disk for software examples.

The following tables show the jumpers setting examples for each mode of DMA:

Option	E4	E5	E6	E7
Channel A No DMA; Channel B No DMA	None	None	None	None

Single Channel DMA (Half Duplex Only):

Ch. A DMA: Ch. 0 Half Duplex: Ch. B No DMA	None	00	None	None
Ch. A DMA: Ch. 1 Half Duplex: Ch. B No DMA	None	11	None	None
Ch. A DMA: Ch. 2 Half Duplex: Ch. B No DMA	None	22	None	None
Ch. A DMA: Ch. 3 Half Duplex: Ch. B No DMA	None	33	None	None

Ch. B DMA: Ch. 0 Half Duplex: Ch. A No DMA	None	None	None	00
Ch. B DMA: Ch. 1 Half Duplex: Ch. A No DMA	None	None	None	11
Ch. B DMA: Ch. 2 Half Duplex: Ch. A No DMA	None	None	None	22
Ch. B DMA: Ch. 3 Half Duplex: Ch. A No DMA	None	None	None	33

Two DMA Channels Selected:

Ch. A DMA Ch. 1 Half Duplex Ch. B DMA Ch. 3 Half Duplex	None	11	None	33
Ch. A DMA Ch. 0 Half Duplex Ch. B DMA Ch. 2 Half Duplex	None	00	None	22

Full Duplex Channel A and B with four DMA Channels:

Ch. A DMA Ch. 1 Receive Data Ch. A DMA Ch. 3 Transmit Data Ch. B DMA Ch. 0 Receive Data Ch. B DMA Ch. 2 Transmit Data	33	11	22	00

Full Duplex Channel A only:

Ch. A DMA Ch. 1 Receive Data Ch. A DMA Ch. 3 Transmit Data	33	11	None	None

E2: Select whether the DMA tri-state drivers are enabled permanently, disabled permanently, or whether the DMA enable control port bit is used to enable the DMA hardware request and acknowledge signals. Moving the jumper to position "N" disables the drivers and no DMA can be performed.

NOTE:

The Power on reset signal resets, or disables the DMA software enable signal.

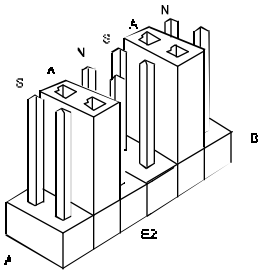


Figure 5: DMA enable header E2 (shown on Factory Default)

S	Selects Software Enable Channel A
A	Selects Always Enable Channel A
N	Selects No DMA Channel A
S	Selects Software Enable Channel B
A	Selects Always Enable Channel B
N	Selects No DMA Channel B

NOTE:

Please refer to Chapter 4 for software bit definitions and examples of DMA driver control.

E3: Selects the interrupt request (IRQ) line for the card. If no interrupt is desired, remove the jumper.

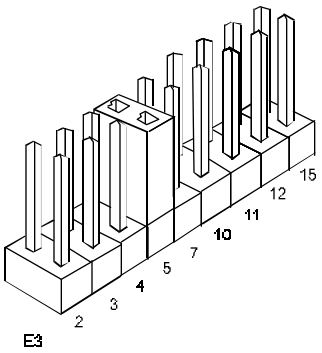


Figure 6: IRQ Header E3 (shown in factory default setting)

E1: "N" indicates the (N)ormal single interrupt mode. Position "M" indicates the inclusion of a 1K ohm pull-down resistor required on one port when sharing interrupts with another card. For shared interrupt mode, set one board to "M" and the other(s) with the jumper removed. This mode allows more than one board to access a single IRQ. Position "T" on E1 enables the DMA Terminal Count Interrupt. Setting this jumper allows the selected DMA channel to generate an interrupt once the DMA Terminal Count has been reached. See Section 4 for the status bit (TC STAT) position and refer to the toolkit disk for software examples.

NOTE:

When using multiple cards on one IRQ in shared mode, be sure that only one port has the “M” jumper set, providing the necessary pull-down resistor.

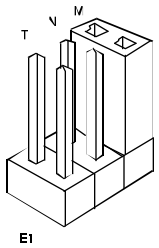


Figure 7: IRQ mode header (shown set in the factory default setting)

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Chapter 4: Technical Description

The ACB4-AT Advanced Communications Board provides the PC/XT/AT with two high speed sync/async ports. The ACB4-AT can be used in a variety of sophisticated communications applications such as SDLC, HDLC, X .25, and high speed async.

Features Include:

- Two Channels of Sync/Async communications using 85230 SCC
- DMA supports data rate greater than 1 million bps (Bits per second)
- Selectable Port Address, IRQ level (2,3,4,5,7,10,11,12,15)
- Selectable DMA Channel (0,1,2 OR 3)
- RS-530/422/485 interface with full modem control
- Supports TD,RD,RTS,CTS,DSR,DCD,DTR,TXC,RXC,LL,RL,TM and TSET signals
- Jumper options for clock source and Input/Output mode
- Software programmable baud rate

The ACB4-AT utilizes the Zilog 85230 Enhanced Serial Communications Controller (ESCC). This chip features programmable baud rate, data format, interrupt control, and DMA control. Refer to the Zilog Micro-communications Handbook or the Serial Communication Controller Technical Reference for details on programming the chip.

RS-422 signal level drivers and receivers are provided on the serial port. The DB-25 male connectors meet the RS-530 specification for RS-530 DTE devices. RS-530 is backwardly compatible with (and is replacing) the RS-449 specification for telecom applications. All of the RS-530 modem control signals provided, including Local Loop-back (LL), Remote Loop-back (RL), and Test Mode (TM). The ACB4-AT also supports the RS-485 communications. The following is a brief summary of the RS-422, RS-530, and RS-485.

RS-422

RS-422 was developed to allow very long distance (5000ft at 9600 baud) communications with virtually error free differential drive characteristics, as opposed to RS-232. The RS-422 interface driver enable signal should be high (or permanently enabled) for normal operation. To permanently enable the driver, remove jumper position "E" on E8 for Channel A or B.

EIA-530

RS-530 compatibility means that RS-422 signal levels are met, and that the pinout of the DB-25 connector is specified. In the past, RS-422 and RS-485 connector pinouts were not standardized. This created a problem when different devices were connected. The EIA (Electronic Industry Association) created the RS-530 specification to detail the pinout. RS-530 is very similar to RS-449, which calls for RS-422 DB-37 connector. The RS-530 is broken into two interfaces: DTE and DCE, much like RS-232. The ACB4-AT has a RS-530 DTE interface. In addition to the asynchronous modem control signals found on standard PC serial port, RS-530 specifies synchronous clock signals, modem test and loop-back signals. The RS-422 driver enable jumpers (marked E) on E8 should be removed, as in RS-422 modes.

RS-485

RS-485 is backwardly compatible with RS-422, however optimized for partyline or multi-drop applications. The output of the RS-422/485 driver is capable of being Active (on) or Tri-State (off). This capability allows multiple PC's (or other RS-422/485 devices) to be connected in a multi-drop bus and selectively polled. Half-duplex two-wire operation is also possible by connecting TX+ to RX+ and TX- to RX- (in the connector hood). The enable to the driver is connected to the SCC Request To Send (RTS) line. This is done by installing the "E" jumpers on E8 for Channels A and B. The unused RS-530 signals can be left disconnected or floating, as they have pull-up/pull-down resistors to provide an ON (or true) condition if not connected.

Control/Status Port

The ACB4-AT occupies eight Input/Output (I/O) addresses. The first four are used by the SCC chip, while the fifth address (Base+4) is the address of the on-board Control/Status Port. This port is used to set the Data Terminal Ready (DTR) signal, and Remote and Local Loop-back (RL and LL) signals on or off, to enable or disable DMA under program control, and to monitor the Data Set Ready (DSR), and Test Mode (TM) input signals from the modem. The following table lists bit positions of the Control/Status port.

Bit	Output Port Bits		Input Port Bits	
0	DTR A	1= ON 0=OFF	DSR A	1=OFF 0=ON
1	DTR B	1= ON 0=OFF	DSR B	1=OFF 0=ON
2	LL A	1= ON 0=OFF	TM A	1=OFF 0=ON
3	RL A	1= ON 0=OFF	SCC INT	1=OFF 0=ON
4	LL B	1= ON 0=OFF	TM B	1=OFF 0=ON
5	RL B	1= ON 0=OFF	TC STAT	1=OFF 0=ON
6	Ch.B DMA Enable SCC Ch. B 1=ON 0=OFF		Ch. B DMA	1=OFF 0=ON
7	Ch.A DMA Enable SCC Ch. A 1=ON 0=OFF		Ch. A DMA	1=OFF 0=ON

NOTE:

Wrtiting a "1" sets the bit "ON", while Reading a "0" indicates that the signal is "On"

Software Examples

Output Function	Program Code	Comment
Turn On Ch. A DTR	Out Base+4, XXXX XXX1	1 Turns DTR A On
Turn On Ch. B DTR	Out Base+4, XXXX XX1X	1 Turns DTR B On
Trun Off Ch. A DTR	Out Base+4, XXXX XXX0	0 Turns DTR A Off
Turn Off Ch. B DTR	Out Base+4, XXXX XX0X	0 Turns DTR B Off
Turn On Ch. A LL	Out Base+4, XXXX X1XX	1 Turns LL A On
Turn Off Ch. A LL	Out Base+4, XXXX X0XX	0 Turns LL A Off
Turn On Ch. A RL	Out Base+4, XXXX 1XXX	1 Turns RL A On
Turn Off Ch. A RL	Out Base+4, XXXX 0XXX	0 Turns RL A Off
Turn On Ch. B LL	Out Base+4, XXX1 XXXX	1 Turns LL B On
Turn Off Ch. B LL	Out Base+4, XXX0 XXXX	0 Turns LL B Off
Turn On Ch. B RL	Out Base+4, XX1X XXXX	1 Turns RL B On
Turn Off Ch. B RL	Out Base+4, XX0X XXXX	0 Turns RL B Off
Enable Ch. B DMA	Out Base+4, X1XX XXXX	1 Turns Ch. B DMA On
Disable Ch. B DMA	Out Base+4, X0XX XXXX	0 Turns Ch. B DMA Off
Enable Ch. A DMA	Out Base+4, 1XXX XXXX	1 Turns Ch. A DMA On
Disable Ch. A DMA	Out Base+4, 0XXX XXXX	0 Turns Ch. A DMA Off

Input Function	Program Code	Comment
Test Ch. A DSR	In Base+4, Mask=0000 0001	1 Indicates DSR Off
Test Ch. B DSR	In Base+4, Mask=0000 0010	0 Indicates DSR is ON
Test Ch. A TM	In Base+4, Mask=0000 0100	1 Indicates TM Off
Test Ch. B TM	In Base+4, Mask=0001 0000	0 Indicates TM is On

The ACB4-AT can be setup to operate using a polling method, interrupts, or to utilize system DMA. The most efficient method is a combination of DMA and interrupts. The ACB4-AT has been optimized to generate an interrupt at the end of a DMA transfer. This will allow for DMA initialization and buffer management to take place at interrupt time and provide a virtually seamless communication channel. If the "T" option on header E1 is selected, an onboard latch will be set when Terminal Count for the selected DMA channel(s) is reached. This latch will cause an interrupt to be generated and program execution will be transferred to the application Interrupt Service Routine (ISR). The DMA Terminal Count Interrupt condition should be reset from the ISR by writing to BASE+5. The value that is written to the I/O location is irrelevant. If your application or driver is interrupting on multiple conditions, reading the Status Register located at Base+4 will determine the source of the interrupt (SCC or DMA Terminal Count generated). Bit D3 in the Status Port corresponds to a SCC generated interrupt and bit D5 corresponds to an interrupt generated by the end of a DMA transfer. Bit D3 can only be set by polling the SCC to determine the interrupt source and required action necessary to reset the interrupt.

NOTE:

Assembly language programs should not do two successive I/O accesses, as this violates the 85230 SCC recovery time specification. Please refer to the 85230 technical reference for more details.

Correct:			Incorrect:		
MOV	DX,	3EOH	MOV	DX,	3EOH
OUT	DX,	AL	OUT	DX,	AL
JMP	$+2		OUT	DX,	AL
OUT	DX,	AL			

Direct Memory Access

Direct Memory Access (DMA) can be used to transfer data at very high rates. This requires additional programming and a very good understanding of the operation of the PC's DMA controller. The software examples provided on diskette demonstrate the setup and use of DMA.

Internal BAUD Rate Generator

The baud rate of the SCC is programmed under software control. The standard oscillator supplied with the board is 7.3728 Megahertz (MHZ). Other values may be substituted to achieve a different baud rate by replacing the oscillator (Y1) with a new part.

P1 Connector Pin-Out

Signal		Name	Pin#	Mode
GND		Ground	7	Input RS-422
RDB	RX+	Receive Positive	16	Input RS-422
RDA	RX-	Receive Negative	3	Input RS-422
CTSB	CTS+	Clear to Send Positive	13	Input RS-422
CTSA	CTS-	Clear to Send Negative	5	Input RS-422
DSRB	DSR+	Data Set Ready Positive	22	Input RS-422
DSRA	DSR-	Data Set Ready Negative	6	Input RS-422
DCDB	DCD+	Data Carrier Detect Positive	10	Input RS-422
DCDA	DCD-	Data Carrier Detect Negative	8	Input RS-422
TDB	TX+	Transmit Positive	14	Output RS-422
TDA	TX-	Transmit Negative	2	Output RS-422
RTSB	RTS+	Request to Send Positive	19	Output RS-422
RTSA	RTS-	Request to Send Negative	4	Output RS-422
DTRB	DTR+	Data Terminal Ready Positive	23	Output RS-422
DTRA	DTR-	Data Terminal Ready Negative	20	Output RS-422
TXCB	TXC+	Transmit Clock Positive	12	Input RS-422
TXCA	TXC-	Transmit Clock Negative	15	Input RS-422
RXCB	RXC+	Receive Clock Positive	9	Input RS-422
RXCA	RXC-	Receive Clock Negative	17	Input RS-422
TSETB	TSET+	Terminal Timing Positive	11	Output RS-422
TSETA	TSET-	Terminal Timing Negative	24	Output RS-422
LL		Local Loop-Back	18	Output (for testing)
RL		Remote Loop-Back	21	Output (for testing)
TM		Test Mode	25	Input (for testing)

RS-530/422/485 Line Termination

Typically, each end of the RS-530/422/485 bus must have line terminating resistors. A 100 ohm resistor is across each RS-530/422/485 input in addition to a 1K ohm pull-up/pull-down combination that bias the receiver inputs.

The RS-530 spec calls for a 100 ohm 1/2 watt resistor between the signal ground and the chassis ground. On the IBM PC, these two grounds are already connected together, therefore the resistor is omitted.

How to remain CE Compliant

In order for machines to remain CE compliant, only CE compliant parts may be used. To keep a chassis compliant it must contain only compliant cards, and for cards to remain compliant they must be used in compliant chassis. Any modifications made to the equipment may affect the CE compliance standards and should not be done unless approved in writing by Industrial Computer Source.

The Model ACB4-AT is designed to be CE Compliant when used in an CE compliant chassis. Maintaining CE Compliance also requires proper cabling and termination techniques. The user is advised to follow proper cabling techniques from sensor to interface to ensure a complete CE Compliant system. Industrial Computer Source does not offer engineering services for designing cabling or termination systems. Although Industrial Computer Source offers accessory cables and termination panels, it is the user's responsibility to ensure they are installed with proper shielding to maintain CE Compliance.

Chapter 5: Specifications

Enviromental Specifications

Specification	Operating	Storage
Temperature Range	0° to 50° C 32° to 122° F	-20° to 70° C -40° to 100° F
Humidity Range	0 to 90% R.H Non-Condensing	0 to 90% R.H Non-Condensing

Performance Specifications

MTBF >150,000 Hours

MTTR <.25 Hours

Manufacturing Specifications

- IPC 610-A Class-III standards adhered to with a 0.1 visual A.Q.L. and 100% Functional Testing.
- Boards are built to U.L. 940VO rating and are 100% Electrically tested. Most boards are solder mask over bare copper.

Power Specifications

Supply Line	+5	+12	-12
Rating (mA)	195 mA	N/A	N/A

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Declaration of Conformity

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Industrial Computer Source declares under its own and full responsibility that the following products are compliant with the protection requirements of the 89/336/EEC directives.

Only specific models listed on this declaration and labeled with the CE logo are CE compliant.

ACB4-AT ACB4-AT/16MHZ

Conformity is accomplished by meeting the requirements of the following European harmonized standards:

EN 50082-1:1992	EMC Generic Immunity Standard
EN 55022:1987	Limits & Methods of measurement of interference characteristics of IT Equipment
EN 60 950	Safety of Information Technology Equipment Including Electrical Business Equipment

Information supporting this declaration is contained in the applicable Technical Construction file available from:

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August 28, 1997
San Diego, CA

Mr. Steven R. Peltier
President & Chief Executive Officer

BUG REPORT

While we have tried to assure this manual is error free, it is a fact of life that works of man have errors. We request you to detail any errors you find on this BUG REPORT and return it to us. We will correct the errors/problems and send you a new manual as soon as available. Please return to:

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Manual Revision: **00750-111-6D**

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