INDUSTRIAL COMPUTER SOURCE

TM

Model ACB6
Product Manual

MANUAL NUMBER :   00750-105-3C

FORWARD

This product manual provides information to install, operate and or program the referenced product(s) manufactured or distributed by Industrial Computer Source. The following pages contain information regarding the warranty and repair policies.

Technical assistance is available at: **1-800-480-0044**.

Manual Errors, Omissions and Bugs: A "Bug Sheet" is included as the last page of this manual. Please use the "Bug Sheet" if you experience any problems with the manual that requires correction.

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In order to receive a full refund on a product purchase price, the product must not have been damaged by the customer or by the common carrier chosen by the customer to return the goods, and the product must be returned complete (meaning all manuals, software, cables, etc.) within 30 days of receipt and in as-new and resalable condition. The **Return Procedure** must be followed to assure prompt refund.

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Chapter 1: Installation

The ACB6 can be installed in any of the PC, XT, or AT expansion slots, except JB on the original IBM XT and Portable. Be sure to set the address and jumper options before installation. To install, remove the PC case, remove the blank metal slot cover, and insert the board. Replace the screw, replace the cover, and installation is complete.

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Chapter 2: Address Selection

The ACB6 occupies 8 consecutive I/O locations. A dip-switch (SW1) is used to set the base address for these locations. Be careful when selecting the base address as some selections conflict with existing PC ports. The following table shows several examples that usually do not cause a conflict.

Address	Binary		Switch Position Settings						
	A9 A0	1	2	3	4	5	6	7
238-23F	1000110XXX	OFF	ON	ON	ON	OFF	OFF	OFF
2A0-2A8	1010100XXX	OFF	ON	OFF	ON	OFF	ON	ON
2E8-2EF	1011101XXX	OFF	ON	OFF	OFF	OFF	ON	OFF
2F8-2FF	1011111XXX	OFF	ON	OFF	OFF	OFF	OFF	OFF
300-308	1100000XXX	OFF	OFF	ON	ON	ON	ON	ON
328-32F	1100101XXX	OFF	OFF	ON	ON	OFF	ON	OFF
3E8-3EF	1111101XXX	OFF	OFF	OFF	OFF	OFF	ON	OFF

Figure 1: Address Selection Table

Typically COM1:-3F8h; COM2:=2F8h; COM3:=3E8h; COM4:=2E8h

The following illustration shows the correlation between the dip-switch setting and the address bits used to determine the base address. In the example below, the address 300 Hex through 307 Hex is selected. 300 Hex = 11 00000XXXX in binary representation.

Figure 2: DIP Switch Illustration

Note that setting the switch "on" or "closed" corresponds to a "0" in the address, while leaving it "off" or "open" corresponds to a "1".

Port Enable/Disable

The ACB6 can be enabled or disabled with switch position 8 on the dip switch. The port is enabled with the switch "On" or "Closed" and disabled when "Off" or "Open."

The relative I/O address of the 85230 registers are as follows:

- Base+O   Channel A Data Port
- Base+1   Channel A Control Port
- Base+2   Channel B Data Port
- Base+3   Channel B Control Port
- Base+4   Board Control/Status Port

Where "Base" is the selected board base address.

Chapter 3: Technical Description

The ACB6 Advanced Communications Board provides the PC/XT/AT with one high speed sync/async ports and one RS-232 port suitable for use as a CSU command port.

Features Include:

• One Channel of Sync/Async communications using 85230 channel A

• SCC channel B asynchronous port for CSU/DSU Command Port

• Selectable Port Address, IRQ level (2-5, 7, 10-12, 15)

• Selectable DMA Channel (0,1,2,3)

• Selectable RS-232, V.35, RS-422/530, MIL 188-C and MIL 188-114 for Channel A of the SCC on a DB-25P.

• Channel A interface supports TD, RD, RTS, CTS, DRS, DCD, TXC, RXC, DTR, RL, and TSET signals on all interfaces and includes SQD on the RS-232 interface.

• RS-232C CSU/DSU Command Port Interface for Channel B of the SCC supports TD, RD, RTS, CTS, DSR, DCD, DTR, RI, signals on a DB-9P Male Connector.

The board occupies eight Input/Output (I/O) addresses. The first four are used by the SCC, while the fifth, sixth, and seventh addresses (Base+4, Base+5, and Base+6) are the addresses of the on-board Control / Status registers. The address at Base+7 is not used. These ports are used to set the Data Terminal Ready (DTR) signals "On" or "Off," to enable or disable DMA and Interrupts under program control, and to monitor the Data Set Ready (DSR), Data Carrier Detect (DCD), Ring Indicator (RI), and Signal Quality Detect (SQD) signals from the modem, as well as determining the source of interrupt.

	BASE+4	BASE+4	BASE+5	BASE+6
BIT	OUTPUT BIT	INPUT BIT	INPUT BIT	INPUT BIT
D0	DTR A-1=ON	DSRA-0=ON	DTRA 0=ON	RS-232=0
D1	DTR B-1=ON	DSRB-0=ON	DTRB 0=ON	V.35=0
D2	X	SQDA-0=ON	DCDA 0=ON	RS-530=0
D3	X	SCCIRQ-0=ON	TCIRQ 0=ON	MIL188=0
D4	X	DCD B-0=ON	SCCIRQ 0=ON	X
D5	X	TCRIQ-0=ON	X	X
D6	IRQ Enable-1=ON	IRQEN-0=ON	X	X
D7	DMA Enable-1=ON	DMEAN-0=ON	X	X

Figure 3: Status and Control Port Bit Definitions

X=Unused Bits

SQD: Signal Quality Detect signal provided by some modems on pin 21 of the DB-25 connector. This signal is provided only when the RS-232 interface is selected.

TCIRQ: Terminal Count IRQ is generated when the DMA controller has transferred all of the programmed number of data bytes, and the DMA transfer is completed.

SCCIRQ: SCC generated interrupt indicating that the 8530 is requesting a data transfer or indicating a status change.

For both Channels A and B, the DCD and RI signals are "OR'ed" together to form the DCD input to the SCC. This is to allow the status change interrupt to generate and IRQ when "Ring" occurs. The assumption is that "Ring" is pulsing active low, and goes back to a high after the "Ring". This will not interfere with DCD, as RI returns high, allowing the program to determine which signal caused the IRQ.

The Terminal Count IRQ is generated by "Anding" Terminal Count (TC) with DMA Acknowledge. The signal is then "Or'ed" with the 8530 INT/ to generate the main bus IRQ signal. Upon interrupt, the Interrupt Service Routine (ISR) can read the status register, look at bit D5 of Base+4, and "O" will be in bit position D5 of Base+4. It can also be determined if the SCC generated the IRQ by reading bit D3 of Base+4. A "0" here indicates an active SCC INT/.

NOTE:

When an IRQ occurs, several conditions may have generated an active interrupt signal. With this in mind, application software should check for all possible conditions.

The TCIRQ latch is cleared by doing a "Dummy Write" to location Base+5. This generates a short pulse to preset the D-latch, causing the IRQ line to return low. The data written during this "Dummy Write" is irrelevant.

Software Considerations

Although interrupts are disabled when the ACB6 is powered on, the TCIRQ latch is not preset. It is advised to reset the TCIRQ latch before enabling interrupts.

The 85230 SCC requires that successive I/O accesses Not Be Made to the SCC as this violates the SCC "Recovery Time." All programs written in Assembly Language and some C compilers should insert a short jump to meet this timing requirement. See below for example:

	Correct		**Incorrect**
•	MOV DX, 3EOH	•	MOV DX,3E0H
•	OUT DX, AL	•	OUT DX, AL
•	JMP $+2	•	OUT DX, AL
•	OUT DX, AL		

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Chapter 4: Option Selection

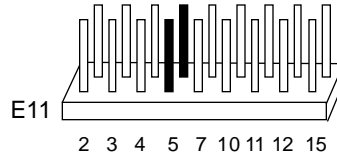E11:   Selects the interrupt request line for the port. If no interrupt is desired, remove the jumper.

E11

2 3 4 5 7 10 11 12 15

Figure 4: Header E11 (IRQ 5 selected)

A B D T N M C E

E9

Figure 5: Header E9 selection (shown set in factory default)

Set jumper to "A: to enable the DMA channel selected on E15. Jumper "B" enables the DMA channel selected on E16. Note that E15 corresponds to the 8530 signal WAIT/REQ and can be used for transmit or receive DMA transfers only. Jumper E16 corresponds to the 8530 signal DTR/WAIT and can be used for transmit DMA transfers only. If you are using the ACB6 in a full duplex DMA situation, set the transmit DMA channel on jumper E16 and the receive DMA channel on jumper E15. Removing the "A" and the "B" jumper will disable both DMA channels.

If the "D" jumper is installed, the DMA enable is controlled through software. If the jumper is installed, the DMA is enabled by setting (1) bit D7 in the Control Register at I/O location Base+4. to disable DMA, reset (0) bit D7 at Base+4. If the jumper is removed DMA is always enabled.

Set jumper to "T" to enable the Terminal Count interrupt. When a DMA transfer is complete, the DMA count register rolls over the 65,535 (FFFF Hex). Once the Count Register reaches this number, the DMA transfer is complete, i.e. the Terminal Count has been reached. The ACB6 card will generate an interrupt at the end of a DMA transfer if this option is selected. The status of the interrupt can be obtained by checking bit D5 in the status register at Base+4. To clear the pending Terminal Count IRQ, read the I/O location at Base+5 and re-initialize the DMA controller.

Set jumper to "N" for single interrupt mode. This setting is the normal setting for most applications.

Set jumper to "M" to include a 1K Ohm resistor needed in "Shared" interrupt mode. Be sure that only one port has the "M" jumper set or that only one resistor is in the circuit.

NOTE:

If two or more ACB6 cards are used in a bus set one jumper "M" and set no jumpers at positions "N" or "M" on the other ACB6 cards..

In most instances the ACB6 will receive both the RXC and TXC clocks from the modem or channel bank. For this reason both the RXC and TXC pins on P1 are always inputs and the SCC RTXC and TRXC pins (Wr11) should be programmed as inputs. If the ACB6 is to receive the TXC input clock on the TXC pin(s) install a jumper at "C".

TSET: The clocks (transmit and receive) for Channel A are supplied to the board by the modem or channel bank. The transmit clock supplied by the modem can be echoed out to the interface connector as Transmit Signal Element Timing (TSET).

If the board is to source a transmit clock, as in modem-less operation, remove jumper at "C" and program the SCC to generate a bit clock on the SCC TRXC pin, which will then be sent out on the TSET pin(s) of P1. The baud rate for the SCC can be set internally in the chip, using a programmed divisor and the oscillator frequency of 7.3728 Megahertz (MHz).

Set jumper to "E" of the EIA-530 (and RS-485) transmit driver is to be enabled by the SCC signal Request To Send (RTS) with the jumper installed RTS enables the driver. Removing the jumper enables the driver regardless of RTS. This jumper should only be installed if you are running the board in a multi-drop polled environment such as RS-485, and you have software that knows how to "Talk" on the RS-485 bus. For normal point-to-point EIA-530 and RS-422, remove the jumper.
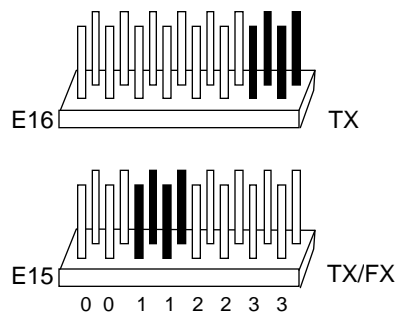
Figure 6: Header E15 & E16

E15 & E16 select DMA mode of operation. Channel A of the SCC will function in half duplex or full duplex DMA modes. Full duplex means that DMA can be used for simultaneous transmit and receive. Half duplex DMA means that you can either transmit, or receive with DMA. The 85230 has two signals that correspond to DMA request signals. WAIT/REQ and DTR/REQ. E15 corresponds to WAIT/REQ and E16 corresponds to DTR/REQ. WAIT/REQ and DTR/REQ can be programmed to serve a DMA request lines by setting the appropriate bits in Write Register 1 and Write Register 14 in the 85230. WAIT/REQ (E15) can be programmed for transmit or receive DMA transfers to DTR/REQ can be programmed for transmit only. Please not that each DMA channel is selected by two jumpers. Only one DMA channel may be selected for each header block.

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Chapter 5: Interface Selection

Interface selection is as easy as installing five dip jumpers (shunts) in the correct sockets. The following table lists the sockets for each of the available interfaces. Please note that all 5 must be set correctly. Also note that each socket is labeled to indicate the interface selection it corresponds to. Please refer to the Silk-screen drawing provided as an aid in locating these positions.

INTERFACE	JUMPERS INSTALLED
RS-232	E10, E8, E5, E1, E17
EIA-530	E4, E13, E12, E1, E17
CCITT V.35	E3, E8, E6, E1, E17
MIL-188-114	E2, E14, E19, E18, E1
MIL-188-C	E2, E14, E17, E18, E19

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Chapter 6: Connector Pinouts

Channel A Pin Definitions

RS-232 Signals

Signal	Name	Pin#	Mode
GND	Ground	7	
RD	Receive Data	3	Input RS-232
CTS	Clear to Send	5	Input RS-232
DSR	Data Set Ready	6	Input RS-232
DCD	Data Carr. Detect	8	Output RS-232
TD	Transmit Data	2	Output RS-232
RTS	Req. to Send	4	Output RS-232
TXC	Transmit Clock	15	Input RS-232
RXC	Receive Clock	17	Input RS-232
TSET	Tx. Sig. Element Tim.	24	Output RS-232
DTR	Data Terminal Ready	20	Output RS-232
RI	Rign Indicator	22	Input RS-232
SQD	Signal Quality Detect	21	Input RS-232

V.35 Signals

Signal	Name	DB-25 Pin	V.35 Pin	Mode
GND	Ground	7	B	
RDB RX+	Receive Positive	10	T	Input V.35
RDA RX-	Receive Negative	11	R	Input V.35
CTS	Clear to Send	5	D	Input RS-232
DSR	Data Set Ready	6	E	Input RS-232
DCD	Data Carr. Detect	8	F	Input RS-232
TDB TX+	Transmit Positive	12	S	Output V.35
TDA TX-	Transmit Negative	13	P	Output V.35
RTS	Request to Send	4	C	Output RS-232
TXCB TXC+	Transmit Clock Pos.	21	AA	Input V.35
TXCA TXC-	Transmit Clock Neg.	23	Y	Input V.35
RXCB RXC+	Receive Clock Pos.	24	X	Input V.35
RXCA RXC-	Receive Clock Neg.	25	V	Input V.35
TSETB TSET+	Ts. Signal Timing Pos.	19	W	Output V.35
TSETA TSET-	Ts. Signal Timing Neg.	18	U	Output V.35
DTR	Data Terminal Ready	20	H	Output RS-232
RI	Ring Indicator	22	J	Input RS-232

EIA-530, RS-422, and MIL-188 Signals

Signal	Name	Pin#	Mode
GND	Ground	7	
RDB RX+	Receive Positive	16	Input
RDA RX-	Receive Negative	3	Input
CTSB CTS+	Clear to Send Pos.	13	Input
CTSA CTS-	Clear to Send Neg.	5	Input
DSRB DSR+	Data Set Ready Pos.	22	Input
DSRA DSR	Data Set Ready Neg.	6	Input
DSDB DCD+	Data Carr. Detect Pos.	10	Input
DCDA DCD-	Data Carr. Detect Neg.	8	Input
TDB TX+	Transmit Positive	14	Output
TDA TX-	Transmit Negative	2	Output
RTSB RTS+	Req. to Send Pos.	19	Output
RTSA RTS-	Req. to Send Neg.	4	Output
DTRB DTR+	Data Term. Ready Pos.	23	Output
DTRA DTR-	Data Term. Ready Neg.	20	Output
TXCB TXC+	Transmit Clock Pos.	12	Input
TXCA TXC-	Transmit Clock Neg.	15	Input
RXCB RXC+	Receive Clock Pos.	9	Input
RXCA RXC-	Receive Clock Neg.	17	Input
TSETB TSET+	Terminal Timing Pos.	11	Output
TSETA TSET-	Terminal Timing Neg.	24	Output
RIA RI-	Ring Indicator Neg.	18	Input
RIB RI+	Ring Indicator Pos.	25	Input

NOTE:

The EIA-530 pinout is adhered to except for the signal Ring Indicator which is not specified by EIA-530.

RS-422/530 Line Termination

Each receiver of the RS-422 / 530 line has a 100 ohm resistor across the input and a 1k ohm pull-up/pull-down combination bias the receiver inputs.

MIL 188-C/MIL 188-114 Selection

Installing jumper E17 will selected MIL 188-C single ended signaling. Removing this jumper enables MIL 188-114 differential operation. Optional slew rate limiting capacitors can be installed at locations C28-C35.

NOTE:

If the Mil 188-114 interface is selected, only the signals marked Positive or + should be connected to your connector hood.

Channel B Pin Definitions

RS-232 SCC Channel B Signals

Signal	Name	Pin#	Mode
GND	Ground	5	
RD	Receive Data	2	Input RS-232
CTS	Clear to Send	8	Input RS-232
DSR	Data Set Ready	6	Input RS-232
DCD	Data Carr. Detect	1	Input RS-232
RI	Ring Indicator	9	Input RS-232
TD	Transmit Data	3	Output RS-232
RTS	Request to Send	7	Output RS-232
DTR	Data Terminal Ready	4	Output RS-232

NOTE: This is the "AT" standard DB-9 style connector

Cable Options

Several cabling options are available including RS-449 adapters and V.35 cables. Please contact Industrial Computer Source Technical Support for more information on cabling options.

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Chapter 7: Specifications

Environmental Specifications

Specification	Operating	Storage
Temperature Range	0° to 50° C 32° to 122° F	-20° to 70° C -40° to 100° F
Humidity Range	0 to 90% R.H Non-Condensing	0 to 90% R.H Non-Condensing

Performance Specifications

MTBF > 150,000 hours

MTTR < .25 hours

Manufacturing Specifications

• IPC 610-A Class-III standards adhered to with a 0.1 visual A.Q.L. and 100% Functional Testing.

• Boards are built to U.L. 94VO rating and are 100% Electrically tested. Boards are Solder Mask over bare Copper or Solder Mask over Tin Nickel.

Power Specifications

Supply Line	+5VDC	-5VDC	-12VDC	+12VDC
Rating (mA)	750	85	15	15

Board Size

The maximum length of the board as measured from the rear board bracket is 13.330". The height of the board as measured from the motherboard edge connector is 4.2". These measurements are held to +/- .010 inches in manufacturing.

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BUG REPORT

While we have tried to assure this manual is error free, it is a fact of life that works of man have errors. We request you to detail any errors you find on this BUG REPORT and return it to us. We will correct the errors/problems and send you a new manual as soon as available. Please return to:

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Product: **ACB6**

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