Model ACB5
Product Manual

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FORWARD

This product manual provides information to install, operate and or program the referenced product(s) manufactured or distributed by Industrial Computer Source. The following pages contain information regarding the warranty and repair policies.

Technical assistance is available at: **1-800-480-0044**.

Manual Errors, Omissions and Bugs: A "Bug Sheet" is included as the last page of this manual. Please use the "Bug Sheet" if you experience any problems with the manual that requires correction.

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> To reduce risk of damage, returns of product must be in an Industrial Computer Source shipping container. If the original container has been lost or damaged, new shipping containers may be obtained from Industrial Computer Source Customer Service at a nominal cost.

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Chapter 1: Installation

The ACB5 can be installed in any of the PC expansion slots, excluding J8 on the “XT” and Portable. Remove the PC case, remove the blank metal slot cover, and insert the board. Replace the screw, replace the case, and installation is complete.

NOTE:

Be sure to set the address and jumper options before installation.

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Chapter 2: Address Selection

The ACB5 occupies 8 consecutive I/O locations. A dip-switch (SW1) is used to set the base address for these locations. Be careful when selecting the base address as some selections conflict with existing PC ports. The following table shows several examples that usually do not cause a conflict.

Address	Binary	Switch Position Settings						
	A9 A0	1	2	3	4	5	6	7
280-287	10 1000 0XXX	OFF	ON	OFF	ON	OFF	ON	ON
2A0-2A7	10 1010 0XXX	OFF	ON	OFF	ON	ON	ON	ON
388-38F	11 1000 1XXX	OFF	OFF	OFF	ON	OFF	ON	OFF
3A0-3A7	11 1010 0XXX	OFF	OFF	OFF	ON	OFF	ON	ON
1A0-1A7	01 1010 0XXX	ON	OFF	OFF	ON	OFF	ON	ON
2F8-2FF	10 1111 1XXX	OFF	ON	OFF	OFF	OFF	OFF	OFF
3F8-3FF	11 1111 1XXX	OFF	OFF	OFF	OFF	OFF	OFF	OFF
320-327	11 0010 0XXX	OFF	OFF	ON	ON	OFF	ON	ON
238-23F	10 0011 1XXX	OFF	ON	ON	ON	OFF	OFF	OFF

Table 2-1: ACB5 Dip-Switch Settings

If you do not see an address in the table that is compatible with your software, you can determine the switch setting for a particular address by using the table below. The following table shows the correlation between the Dip-switch Setting and the Address Bits used to determine the Base Address. In the example below, the address 300 Hex through 307 hex is selected. 300 Hex = 11 000 0XXX in Binary Representation

Switch Position	Address Line	Example: 300 Hex	Switch
1	A9	1	OFF
2	A8	1	OFF
3	A7	0	ON
4	A6	0	ON
5	A5	0	ON
6	A4	0	ON
7	A3	0	ON

Table 2-2: ACB5 Dip-Switch Settings

Note that setting the switch “on” or “closed” corresponds to a “0” in the address, while leaving it “off” or “open” corresponds to a “1”.

The relative I/O address of the ACB5 registers are as follows:

- Base+0 Channel A Data Port
- Base+1 Channel A Control Port
- Base+2 Channel B Data Port
- Base+3 Channel B Control Port
- Base+4 Board Control/Status Port

Where “Base” is the selected board base address.

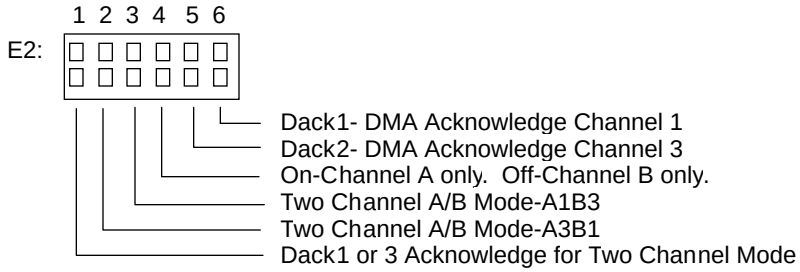
Chapter 3: Option Selection

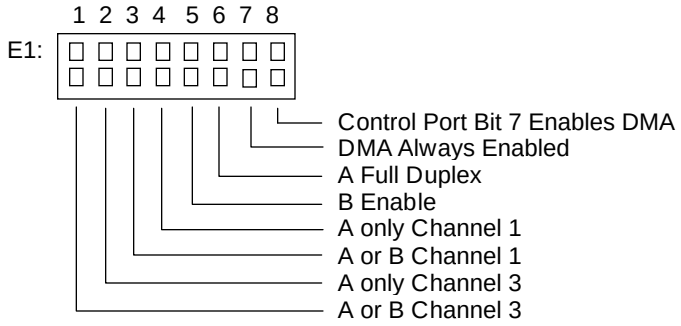
The ACB5 contains several jumper straps which must be set for proper operation.

E1 and E2: Selects DMA Mode of Operation. Channel A of the SCC can be run in Half Duplex or Full Duplex DMA. Full Duplex means that the DMA can be used for simultaneous transmit and receive. Half Duplex DMA means that you can either transmit, or receive with DMA. You can use both Channels A and B, in Half Duplex Mode, to transmit or receive, but not at the same time. The various options and E2 and E1 jumper settings are as follows.

NOTE:

If the DMA is not used, remove all of the jumpers on E1 and E2.



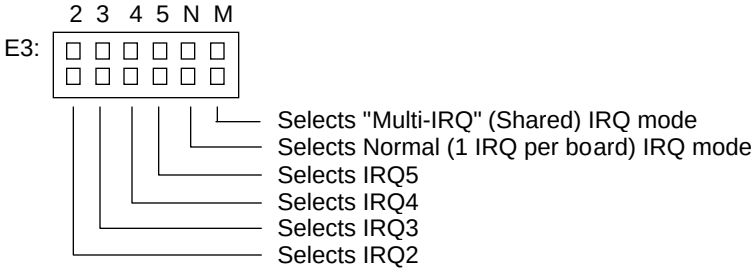


E1 Positions 7 and 8: selects whether the DMA Tri-State Drivers are enabled permanently, or whether the DMA enable control port bit is used to enable the DMA hardware request and acknowledge signals. Removing the jumper disables the driver and no DMA can be performed. Note that the power on reset signals resets, or disables the DMA enable signal.

Option	Jumpers on E2	Jumpers on E1	Program 8530
No DMA Channel A or B	None	None	None
Single Channel DMA (Half Duplex only)			
CH A DMA CH 1 Half Duplex CH B No DMA	4,6	4	WAIT/REQ A
CH A DMA CH 3 Half Duplex CH B No DMA	4,5	2	WAIT/REQ A
CH B DMA CH 1 Half Duplex CH A No DMA	6 only	3,5	WAIT/REQ A
CH B DMA CH 3 Half Duplex CH A No DMA	5 only	1,5	WAIT/REQ A
Both DMA Channels (1 and 3) Selected			
CH A DMA CH 1 Half Duplex CH B DMA CH 3 Half Duplex	1,3	1,4,5	WAIT/REQ A WAIT/REQ B
CH A DMA CH 3 Half Duplex CH B DMA CH 1 Half Duplex	1,2	2,3,5	WAIT/REQ A WAIT/REQ B
Full Duplex Channel A with both DMA Channels 1 and 3			
CH A DMA CH 1 Receive Data CH A DMA CH 3 Transmit Data	1,4	1,4,6	WAIT/REQ A DTR/REQ A
CH A DMA CH 3 Receive Data CH A DMA CH 1 Transmit Data	1,4	2,3,6	WAIT/REQ A DTR/REQ A

Table 3-1: Channels and Jumpers

E3: selects the interrupt request line for the port. The diagram below shows which IRQ signal corresponds to which jumper position. If no interrupt is desired, remove the jumper. The factory default setting for E3 is" "5" and "M".



EPROM Usage

The EPROM socket on the ACB5 is provided for convenience only and does not affect the communcation functions of the board in any way. If the Eprom is not used, the socket should be disabled (dip-switch SW2 position 5 off). The following table shows several EPROM base address examples.

The EPROM is a 27128 device occupying 16K bytes of memory at or obove C800 Hex to be recognized by the PC on boot up. Address lines A19, and A18 are always a binary 1, forcing a selection of C000 Hex or greater.

Address	Address			Switch position setting (SW1)				
	A17	A16	A15	A14	1	2	3	4
C000-C3FF	0	0	0	0	ON	ON	ON	ON
C400-C7FF	0	0	0	1	ON	ON	ON	OFF
C800-C9FF	0	0	1	0	ON	ON	OFF	ON
D000-D3FF	0	1	0	0	ON	OFF	ON	ON
D4000-D7FF	0	1	0	1	ON	OFF	ON	OFF
D800-DBFF	0	1	1	0	ON	OFF	OFF	ON
E000-E3FF	1	0	0	0	OFF	ON	ON	ON
E400-E7FF	1	0	0	1	OFF	ON	ON	OFF

Table 3-2: EPROM Address Examples

Note: Some "AT" class machines cannot use address E000 and above.

Switch position 5 enables and disables the EPROM socket. The default setting is with the EPROM socket disabled. The ACB5 will be shipped with the dip-switch in the configuration illustrated in Figure 3-2.

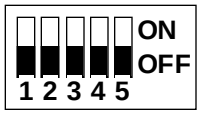


Figure 3-1: Dip-Switch Illustration (SW2)

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Chapter 4: Technical Description

ACB5 Specifications

The ACB5 Advanced Communications Board provides the PC/XT/AT with two high speed sync/async ports. The ACB5 can be used in a variety of sophisticated communications applications such as SDLC, HDLC, X .25, and high speed async.

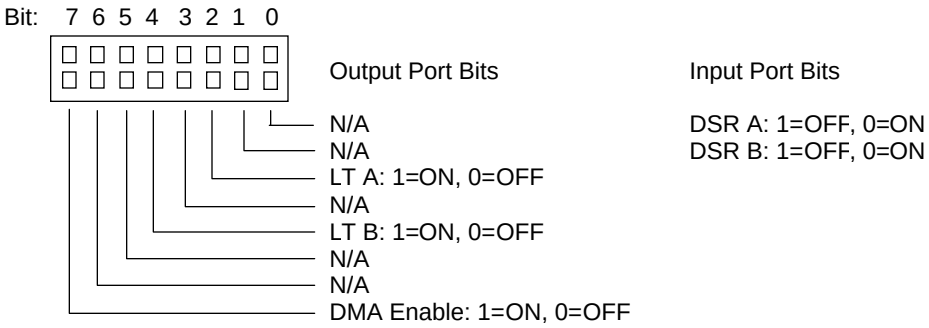
Features Include:

- Two Channels of Sync/Async communications using 85230 SCC
- DMA supports data rate greater than 1 million bps (Bits per second)
- Selectable Port Address, IRQ level (2,3,4,5) and DMA Channel (1 or 3)
- V.35 interface with full modem control
- Supports TD, RD, RTS, CTS, DRS, TXC, RXC, and LT signals.
- On-Board EPROM socket (16K or 128K byte)
- Software programmable baud rate

The ACB5 utilizes the Zilog 85230 Enhanced Serial Communications Controller (ESCC). This chip features programmable baud rate, data format, interrupt control, and DMA control. Refer to the Zilog Micro-communications Handbook or the Serial Communication Controller Technical Reference for details on programming the chip.

CCIT V.35

The Comite Consultatif Internationale de Telegraphie et Telephonie also known as the CCIT is the agency that set the V.35 standard. V.35 specifies an electrical, mechanical, and physical interface that is used extensively by high-speed digital carriers such as AT&T Dataphone Digital Service (DDS). CCIT V.35 is an international standard that is often referred to as "Data Transmission at 48 Kbps Using 60 - 108 KHz Group-Band Circuits." CCIT V.35 electrical characteristics are a combination of unbalanced voltage and balanced current mode signals. Data and clock signals are balanced current mode circuits. These circuits typically have voltage levels from 0.5 Volts to -0.5 Volts (1 Volt differential). The modem control signals are unbalanced signals and are compatible with RS-232. The physical connector is a 34-pin connector that supports 24 data, clock and control signals. The physical connector is defined in the ISO-2593 standard. CCIT V.35 is implemented with both DTE and DCE interfaces, the ACB5 is implemented using the DTE interface. The ACB5 will not generate a clock signal without a modification, because the CCIT V.35 specification does not specify a clock output signal for a V.35 DTE. If an output clock signal is required for the V.35 interface, please call Industrial Computer Source's Technical Support. The ACB5 is compatible with CCIT V.36 and V.37.



Function	Program Code	Comment
Turn ON CH A LT	Out Base+4, XXXX X1XX	1 Turns LT ON
Turn ON CH B LT	Out Base+4, XXX1 XXXX	0 Turns LT OFF
Turn OFF CH A LT	Out Base+4, XXXX X0XX	1 Turns LT ON
Turn OFF CH B LT	Out Base+4, XXX0 XXXX	0 Turns LT OFF
Enable DMA Drivers	Out Base+4, 1XXX XXXX	1 Turns DMA ON
Disable DMA Drivers	Out Base+4, 0XXX XXXX	0 Turns DMA OFF
Test CH A DSR	In Base+4, MASK=0000 0001	1 Means DSR OFF
Test CH B DSR	In Base+4, MASK=0000 0010	0 Means DSR ON

Table 4-1: ACB5 Program Code

Note that normal programming technique would include keeping a memory image to the output port control word and then setting or resetting the appropriate bits only, so as not to alter any other port bits while changing a bit.

NOTE:

Assembly language programs should not do two successive I/O accesses, as this violates the 85230 ESCC recovery time specification. Please refer to the 85230 technical reference for more details.

Correct	Incorrect
• MOV DX, 03EOH	• MOV DX, 03E0H
• OUT DX, AL	• OUT DX, AL
• JMP SHORT, $+2	• OUT DX, AH
• OUT DX, AH	

Direct Memory Access (DMA) can be used to transfer data at very high rates. This requires extensive programming and a very good understanding of the operation of the PC hardware. The software examples provided on diskette demonstrate the setup and use of DMA. Refer to the ACB Toolkit software for applications examples (with source code) to help in your initial software development.

The clocks (Transmit and Receive) are supplied to the board by the modem or channel bank. The Buad rate can be set internally in the chip if desired. The oscillator supplied with the board is 7.3728 megahertz (MHz). Other values may be substituted to achieve a deferent Baud rate.

Signal Name			DB-15 Pin#	V.35 Pin #	Mode
GND	Ground		8	B	
RDB	RX+	Receive Positive	4	T	Input V.35
RDA	RX-	Receive Negative	11	R	Input V.35
CTS		Clear to Send	5	D	Input RS-232
DSR		Data Set Ready	6	E	Input RS-232
DCD		Data Carr. Detect	7	F	Input RS-232
TDB	TX+	Transmit Positive	2	S	Output V.35
TDA	TX-	Transmit Negative	9	P	Output V.35
RTS		Req. to Send	3	C	Output RS-232
TXCB	TXC+	Transmit Clock Pos.	12	AA	Input V.35
TXCA	TXC-	Transmit Clock Neg.	10	Y	Input V.35
RXCB	RXC+	Receive Clock Pos.	13	X	Input V.35
RXCA	RXC-	Receive Clock Neg.	14	V	Input V.35
LT		Line test	15	K	Output for Test

Table 4-2: Transmit and Receive

How to remain CE Compliant

In order for machines to remain CE compliant, only CE compliant parts may be used. To keep a chassis compliant it must contain only compliant cards, and for cards to remain compliant they must be used in compliant chassis. Any modifications made to the equipment may affect the CE compliance standards and should not be done unless approved in writing by Industrial Computer Source.

The Model ACB5 is designed to be CE Compliant when used in an CE compliant chassis. Maintaining CE Compliance also requires proper cabling and termination techniques. The user is advised to follow proper cabling techniques from sensor to interface to ensure a complete CE Compliant system. Industrial Computer Source does not offer engineering services for designing cabling or termination systems. Although Industrial Computer Source offers accessory cables and termination panels, it is the user's responsibility to ensure they are installed with proper shielding to maintain CE Compliance.

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ACB5

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EN 55022:1987	Limits & Methods of measurement of interference characteristics of IT Equipment
EN 60 950	Safety of Information Technology Equipment Including Electrical Business Equipment

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August 28, 1997
San Diego, CA

Mr. Steven R. Peltier
President & Chief Executive Officer

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