INDUSTRIAL COMPUTER SOURCE®

Model ACB3 & ACB3/SP
Product Manual

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FORWARD

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Chapter 1: Introduction

Overview

The Model ACB3 provides the PC with two high speed RS-232 synchronous / asynchronous ports. The ACB3 can be used in a variety of sophisticated communications applications such as SDLC, HDLC, X.25, Bi-Sync and high speed async. The Model ACB3/SP provides a single high speed RS-232 sync/async port.

What's Included

The ACB3 is shipped with the following items. If any of these items are missing or damaged, contact the supplier.

- ACB3 Serial Interface Adapter
- 3.5" ACB Developers Toolkit Diskette
- Channel B Interface Cable
- User Manual

Factory Default Settings

The ACB3 factory default settings are as follows:

Base Address	DMA Channels	IRQ
238	Channel A / B Half Duplex DMA	5

To install the ACB3 using factory default settings, refer to the section on Installation.

For your reference, record installed ACB3 settings below:

Base Address	DMA Channels	IRQ

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Chapter 2: Card Setup

The ACB3 contains several jumper straps for each port which must be set for proper operation.

Address Selection

The ACB3 occupies 8 consecutive I/O locations. A DIP-switch (SW2) is used to set the base address for these locations. The ACB3 can reside in any I/O location between 100 and 3F8 Hex. Be careful when selecting the base address as some selections conflict with existing PC ports. The following table shows several examples that usually do not cause a conflict.

Address	**Binary**	**Switch Position Settings**						
	A9 A0	1	2	3	4	5	6	7
238-23F	1000111XXX	OFF	ON	ON	ON	OFF	OFF	OFF
280-288	1010000XXX	OFF	ON	OFF	ON	ON	ON	ON
2A0-2A8	1010100XXX	OFF	ON	OFF	ON	OFF	ON	ON
2E8-2EF	1011101XXX	OFF	ON	OFF	OFF	OFF	ON	OFF
300-308	1100000XXX	OFF	OFF	ON	ON	ON	ON	ON
328-32F	1100101XXX	OFF	OFF	ON	ON	OFF	ON	OFF
3E8-3EF	1111101XXX	OFF	OFF	OFF	OFF	OFF	ON	OFF

Figure 1: Address Selection Table

The following illustration shows the correlation between the DIP-switch setting and the address bits used to determine the base address. In the example below, the address 300 Hex through 307 Hex is selected. 300 Hex = 11 0000 0XXX in binary representation.

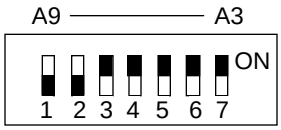


Figure 2: DIP-switch Illustration

Note: Setting the switch "On" or "Closed" corresponds to a "0" in the address, while leaving it "Off" or "Open" corresponds to a "1".

The relative I/O address of the **S**erial **C**ommunication **C**ontroller (SCC) registers is as follows:

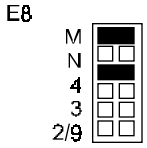
Base+0 Channel A Data Port
Base+1 Channel A Control Port
Base+2 Channel B Data Port
Base+3 Channel B Control Port
Base+4 ACB3 Control/Status Port

Where "Base" is the selected base address.

IRQ Selection (Header E8)

The ACB3 has an interrupt selection jumper which should be set prior to use if an interrupt is required by your application software. Consult the user manual for the application software being used to determine the proper setting.

Positions "**M**" & "**N**" allow the user to select a single interrupt per port mode or a shared interrupt mode. The "**N**" selects the single interrupt per port mode. The "**M**" selects the shared interrupt mode, which allows more than one port to access a single IRQ, and indicates the inclusion of a 1K ohm pull-down resistor required on one port when sharing interrupts.



M	Selects "Multi-IRQ" (Shared) IRQ Mode
N	Selects Normal (1 IRQ Per Board) IRQ Mode
5	Selects IRQ5
4	Selects IRQ4
3	Selects IRQ3
2/9	Selects IRQ2/9

Figure 3: Header E8, IRQ Selection (Shown in Factory Default)

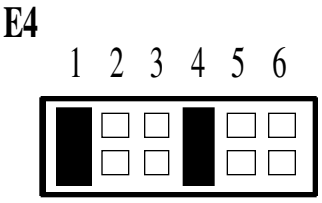
Note: The actual silk-screen for the ACB3 may have a "2" in place of the IRQ "2/9" selection.

DMA Options

Headers E4 and E5 select the **D**irect **M**emory **A**ccess (DMA) mode of operation for the ACB3. Channel A of the SCC can operate in either half-duplex or full duplex DMA mode. Full duplex DMA can transmit and receive data simultaneously. Half-duplex DMA can transmit or receive data, but not in both directions simultaneously.

Note: If DMA is not used, remove all of the jumpers on E4 and E5.

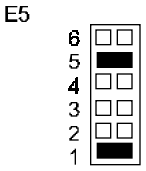
Header E4



1 DACK 1 Or 3 Acknowledge For Two Channel Mode
2 Two Channel A/B Mode A3B1
3 Two Channel A/B Mode A1B3
4 On = Ch. A Only / Off = Ch. B Only
5 DACK 3 DMA Acknowledge Channel 3
6 DACK 1 DMA Acknowledge Channel 1

Figure 4: Header E4 (Factory Default Settings)

Header E5

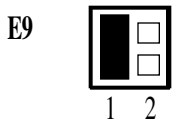


6 SCC Channel A, DMA Channel 1 & 3 for Full Duplex Transfers
5 SCC Channel B Enable for Half Duplex DMA Transfers
4 SCC Channel A only can use DMA Channel 1
3 SCC Channel A or B can use DMA Channel 1
2 SCC Channel A only can use DMA Channel 3
1 SCC Channel A or B can use DMA Channel 3

Figure 5: Header E5 (Factory Default)

Header E9

Positions 1 and 2 of Header E9 enable or disable DMA operation. A jumper "ON" position 1 permanently enables the DMA tri-state drivers. A jumper "ON" position 2 places DMA under software control via the DMA enable control port bit (located at Base+4). **Removing the jumper disables the drivers, and no DMA can be performed.**



1 DMA Tri-State drivers permanently enabled

2 DMA Tri-State drivers enabled by status / control port bit 7

Figure 6: Header E9 (Factory Default)

Note: The power-on reset signal disables the DMA enable signal. A jumper placed in position 1 of E9 will override any software use of the DMA enable/disable status port bit.

Commonly Used DMA Jumper Options

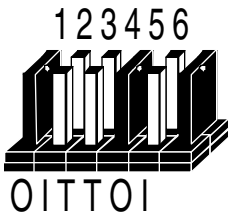
Option	Jumpers on E4	Jumpers on E5	Program 8530
No DMA	None	None	N/A
Single Channel DMA (Half Duplex only)			
CH A DMA CH 1 Half Duplex CH B No DMA	4,6	4,5	WAIT/REQ A
CH A DMA CH 1 Half Duplex CH B No DMA	4,5	2,5	WAIT/REQ A
CH B DMA CH 1 Half Duplex CH B No DMA	6 only	3,5	WAIT/REQ B
CH B DMA CH 1 Half Duplex CH A No DMA	5 only	1,5	WAIT/REQ B
Both DMA Channels (1 and 3) Selected:			
CH A DMA CH 1 Half Duplex CH B DMA CH 3 Half Duplex	1,3	1,4,5	WAIT/REQ A WAIT/REQ B
CH A DMA CH 3 Half Duplex CH B DMA CH 1 Half Duplex	1,2	2,3,5	WAIT/REQ A WAIT/REQ B
Full Duplex using both DMA Channels 1 and 3			
CH A DMA CH 1 Receive Data CH A DMA CH 3 Transmit Data	1,4	1,4,6	WAIT/REQ A DTR/REQ A
CH A DMA CH 3 Receive Data CH A DMA CH 1 Transmit Data	1,4	2,3,6	WAIT/REQ A DTR/REQ A

Figure 7: Commonly Used DMA Options

Remember that E9 positions 1 and 2 enable or disable DMA operation.

Headers E3 and E6

Headers E3 and E6 set the input/output clock modes for the transmit clock (TXC), as well as the RS-485 enable/disable. E3 sets the clock mode for the SCC Channel B (Port 2), while E6 sets the clock mode for the SCC channel A (Port 1).



1 Transmit Clock Output (TXC OUT)*

2 Transmit Clock Input (TXC IN)

3 Terminal Timing - Source from SCC's TRXC pin or the input to TXC pin echoed to DB-25 pin 24

4 Terminal Timing - The input to RXC pin is echoed to DB-25 pin 24

5 Not Used

6 Receive Clock Input**

Figure 8 - Header E3 and E6 Clock Input/Output Modes

*Factory default

**These jumpers are always configured in this manner and should not be removed or replaced.

Note: The TXC pins (12 and 15) can be jumpered as either an input or an output. The TSET pins (11 and 24) will always echo the TXC pins, regardless of whether the TXC pins are selected as an input or an output.

Headers E2 and E10

Headers E2 & E10 select the input/output clock modes (in conjunction with Headers E3 and E6) for the receive clock (RXC) and transmit clock (TXC) pins on the DB-25 connector (pins 15 & 17). E2 sets the clock mode for the SCC Channel B (Port 2), while E10 sets the clock mode for the SCC Channel A (Port 1).

Note: The jumper for pin 17 must always be chosen as an input. It cannot be selected as an output as the SCC will not allow the RTXC pin to be programmed as an output.

E2 & E10:

O	Transmit Clock Output (15)
I	Transmit Clock Input (15)
O	N/A
I	Receive Clock Input (17)

Figure 9: Header E2 and E10 (shown in factory default)

Chapter 3: Installation

The ACB3 can be installed in any of the PC expansion slots. The **ACB3** contains several jumper straps for each port which must be set for proper operation.

1. Turn off PC power. Disconnect the power cord.
2. Remove the PC case cover.
3. Locate two available slots and remove the blank metal slot covers.
4. Install the Channel B cable into Box Header E1. This cable is keyed to prevent improper installation. Gently insert the ACB3 into the slot. Make sure that the adapter is seated properly. Attach the Channel B cable to the adjacent slot with the retaining screw. (If Channel B of the ACB3 is not used, the adapter cable is not required).
5. Replace the cover.
6. Connect the power cord.

Installation is complete.

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Chapter 4: Technical Description

The ACB3 utilizes the Zilog 85230 Enhanced **S**erial **C**ommunications **C**ontroller (SCC). This chip features programmable baud rate, data format and interrupt control, as well as DMA control. Refer to the SCC Users Manual for details on programming the SCC.

Features

- Two channels of sync/async communications using 85230 chip
- DMA supports data rate greater than 1 million bps (bits per second)
- Selectable port address, IRQ level (2/9,3,4,5), and DMA channel (1 or 3)
- Jumper options for clock source
- Software programmable baud rate

Product Enhancements

The baud rate of the SCC is programmed under software control. The standard oscillator supplied with the board is 7.3728 MHz. However, other oscillator values can be substituted to achieve different baud rates.

Programming The ACB3 Control/Status Port

The ACB3 occupies eight **I**nput/**O**utput (I/O) addresses. The first four are used by the SCC chip, while the fifth address (Base+4) is the address of the on-board **Control/Status Port.** This port is used to set the **D**ata **T**erminal **R**eady (DTR) signal, to enable or disable DMA under program control, and to monitor the **D**ata **S**et **R**eady (DSR) input signals from the modem. The following table lists bit positions of the Control/Status port.

Bit	Output Port Bits		Input Port Bits	
0	DTR A	1=On, 0=Off	DSR A	1=On, 0=Off
1	DTR B	1=On, 0=Off	DSR B	1=On, 0=Off
7	DMA Enable	1=On, 0=Off	Not Used	

Figure 10: Status/Control Register Bit Definitions

Software Examples

Function	Program Bits
Turn On CH A DTR	Out Base+4, XXXX XXX1
Turn On CH B DTR	Out Base+4, XXXX XX1X
Turn Off CH A DTR	Out Base+4, XXXX XXX0
Turn Off CH B DTR	Out Base+4, XXXX XX0X
Enable DMA Drivers	Out Base+4, XXXX XXXX
Disable DMA Drivers	Out Base+4, 0XXX XXXX
Test CH A DSR	In Base+4, Mask=0000 0001
Test CH B DSR	In Base+4, Mask=0000 0010

Figure 11: Status Register Examples

Note: Assembly language programs should not perform two successive I/O accesses, which violates the 85230 SCC recovery time specification. Please refer to the 85230 technical reference for more details.

Correct:

```
MOV DX,3E0H
OUT DX,AL
JMP $+2
OUT DX,AL
```

Incorrect:

```
MOV DX,3E0H
OUT DX,AL
OUT DX,AL
```

Connector P1 and P2 Pin Assignments

Signal	Name	Pin#	Mode
GND	Ground	7	
RD	ReceiveData	3	Input
CTS	Clear to Send	5	Input
DSR	Data Set Ready	6	Input
DCD	Data Carrier Detect	8	Inputt
TD	Transmit Data	2	Output
RTS	Request To Send	4	Output
TXC	Transmit Clock	15	Input/Output
RXC	Receive Clock	17	Input
TSET	Tx. Signal Element Timing	24	Output
DTR	Data Terminal Ready	20	Output

Figure 12: Connector P1 and P2 Pin Assignments

How to remain CE Compliant

In order for machines to remain CE compliant, only CE compliant parts may be used. To keep a chassis compliant it must contain only compliant cards, and for cards to remain compliant they must be used in compliant chassis. Any modifications made to the equipment may affect the CE compliance standards and should not be done unless approved in writing by Industrial Computer Source.

The Model ACB3 is designed to be CE Compliant when used in an CE compliant chassis. Maintaining CE Compliance also requires proper cabling and termination techniques. The user is advised to follow proper cabling techniques from sensor to interface to ensure a complete CE Compliant system. Industrial Computer Source does not offer engineering services for designing cabling or termination systems. Although Industrial Computer Source offers accessory cables and termination panels, it is the user's responsibility to ensure they are installed with proper shielding to maintain CE Compliance.

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Chapter 5: Specifications

Environmental Specifications

Specification	Operating	Storage
Temperature Range	0° to 50° C 32° to 122° F	-20° to 70° C -40° to 158° F
Humidity Range	10 to 90% R.H Non-Condensing	10 to 90% R.H Non-Condensing

Power Consumption

Supply Line	+5 VDC
Rating	195 mA

Mean Time Between Failures (MTBF)

Greater than 150,000 hours. (Calculated)

Physical Dimensions

Board length	4.9 inches	(12.466 cm)
Board Height including Goldfingers	4.2 inches	(10.668 cm)
Board Height excluding Goldfingers	3.9 inches	(9.906 cm)

Note: Please see Appendix G for board layout and dimensions.

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Appendix A: Troubleshooting

An ACB Developers Toolkit Diskette is supplied with the ACB adapter and will be used in the troubleshooting procedures. By using this diskette and following these simple steps, most common problems can be eliminated without the need to call Technical Support.

1. Identify all I/O adapters currently installed in your system. This includes your on-board serial ports, controller cards, sound cards etc. The I/O addresses used by these adapters, as well as the IRQ (if any) should be identified.
2. Configure your adapter so that there is no conflict with currently installed adapters. No two adapters can occupy the same I/O address.
3. Make sure the adapter is using a unique IRQ. While the adapter does allow the sharing of IRQ's, many other adapters (i.e. SCSI adapters & on-board serial ports) do not. The IRQ is typically selected via an on-board header block. Refer to the section on Card Setup for help in choosing an I/O address and IRQ.
4. Make sure the adapter is securely installed in a motherboard slot.
5. Use the supplied diskette and User Manual to verify that the adapter is configured correctly. The supplied diskette contains a diagnostic program "SSDACB" that will verify if an adapter is configured properly. This diagnostic program is written with the user in mind and is easy to use. Refer to the "UTIL.TXT" file found in the \UTIL sub-directory on the supplied diskette for detailed instructions on using "SSDACB".

The following are known I/O conflicts:

- The 278 and 378 settings may conflict with your printer I/O adapter.
- 3B0 cannot be used if a Monochrome adapter is installed.
- 3F8-3FF is typically reserved for COM1:
- 2F8-2FF is typically reserved for COM2:
- 3E8-3EF is typically reserved for COM3:
- 2E8-2EF is typically reserved for COM4:. This is a valid setup option for the ACB3**.** However, since only 10 address lines are actually decoded, a possible conflict with an advanced video card emulating the IBM XGA adapter (8514 register set) may occur.

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Appendix B: Electrical Interface

RS-232

Quite possibly the most widely used communication standard is RS-232. This implementation has been defined and revised several times and is often referred to as RS-232 or EIA/TIA-232. It is defined by the EIA as the Interface between Data Terminal Equipment and Data Circuit- Terminating Equipment Employing Serial Binary Data Interchange. The mechanical implementation of RS-232 is on a 25 pin D sub connector. The IBM PC computer defined the RS-232 port on a 9 pin D sub connector and subsequently the EIA/TIA approved this implementation as the EIA/TIA-574 standard. This standard is defined as the 9-Position Non-Synchronous Interface between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange. Both implementations are in wide spread use and will be referred to as RS-232 in this document. RS-232 is capable of operating at data rates up to 20 Kbps at distances less than 50 ft. The absolute maximum data rate may vary due to line conditions and cable lengths. RS-232 often operates at 38.4 Kbps over very short distances. The voltage levels defined by RS-232 range from -12 to +12 volts. RS-232 is a single ended or unbalanced interface, meaning that a single electrical signal is compared to a common signal (ground) to determine binary logic states. A voltage of +12 volts (usually +3 to +10 volts) represents a binary 0 (space) and -12 volts (-3 to -10 volts) denotes a binary 1 (mark). The RS-232 and the EIA/TIA-574 specification defines two type of interface circuits, Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). The adapter is a RS-232 Synchronous DTE interface.

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Appendix C: Direct Memory Access

In many instances it is necessary to transmit and receive data at greater rates than would be possible with simple port I/O. In order to provide a means for higher rate data transfers, a special function called **D**irect **M**emory **A**ccess (DMA) was built into the original IBM PC. The DMA function allows the ACB3 (or any other DMA compatible interface) to read or write data to or from memory without using the Microprocessor. This function was originally controlled by the Intel 8237 DMA controller chip, but may now be a combined function of the peripheral support chip sets (i.e. Chips & Technology or Symphony chip sets).

During a DMA cycle, the DMA controller chip is driving the system bus in place of the Microprocessor providing address and control information. When an interface needs to use DMA, it activates a DMA request signal (DRQ) to the DMA controller, which in turn sends a DMA hold request to the Microprocessor. When the Microprocessor receives the hold request it will respond with an acknowledge to the DMA controller chip. The DMA controller chip then becomes the owner of the system bus providing the necessary control signals to complete a Memory to I/O or I/O to Memory transfer. When the data transfer is started, an acknowledge signal (DACK) is sent by the DMA controller chip to the ACB3. Once the data has been transferred to or from the ACB3, the DMA controller returns control to the Microprocessor.

To use DMA with the ACB3 requires a thorough understanding of the PC DMA functions . The ACB Developers Toolkit demonstrates the setup and use of DMA with several source code and high level language demo programs. Please refer to the SCC User's Manual for more information.

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Appendix D: Asynchronous and Synchronous Communications

Serial data communications implies that individual bits of a character are transmitted consecutively to a receiver that assembles the bits back into a character. Data rate, error checking, handshaking, and character framing (start/stop bits or sync characters) are pre-defined and must correspond at both the transmitting and receiving ends. The techniques used for serial communications can be divided two groups, *asynchronous* and *synchronous*.

When contrasting asynchronous and synchronous serial communications, the fundamental differences deal with how each method defines the beginning and end of a character or group of characters. The method of determining the duration of each bit in the data stream is also an important difference between asynchronous and synchronous communications. The remainder of this section is devoted to detailing the differences between character framing and bit duration implemented in asynchronous and synchronous communications.

Asynchronous Communications

Asynchronous communications is the standard means of serial data communication for PC compatibles and PS/2 computers. The original PC was equipped with a communication or COM: port that was designed around an 8250 **U**niversal **A**synchronous **R**eceiver **T**ransmitter (UART). This device allows asynchronous serial data to be transferred through a simple and straightforward programming interface. Character boundaries for asynchronous communications are defined by a starting bit followed by a pre-defined number of data bits (5, 6, 7, or 8). The end of the character is defined by the transmission of a pre-defined number of stop bits (usual 1, 1.5 or 2). An extra bit used for error detection is often appended before the stop bits.

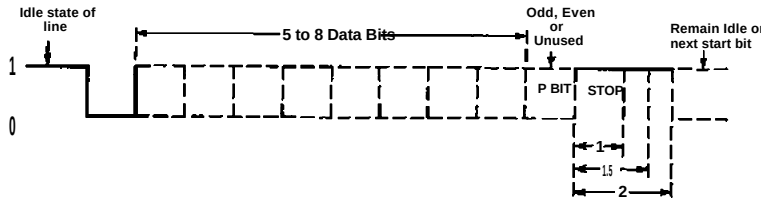

Figure 13: Asynchronous Communications Bit Diagram

This special bit is called the parity bit. Parity is a simple method of determining if a data bit has been lost or corrupted during transmission. There are several methods for implementing a parity check to guard against data corruption. Common methods are called (E)ven Parity or (O)dd Parity. Sometimes parity is not used to detect errors on the data stream. This is referred to as (N)o parity. Because each bit in asynchronous communications is sent consecutively, it is easy to generalize asynchronous communications by stating that each character is wrapped (framed) by pre-defined bits to mark the beginning and end of the serial transmission of the character. The data rate and communication parameters for asynchronous communications have to be the same at both the transmitting and receiving ends. The communication parameters are baud rate, parity, number of data bits per character, and stop bits (i.e. 9600,N,8,1).

Synchronous Communications

Synchronous Communications is used for applications that require higher data rates and greater error checking procedures. Character synchronization and bit duration are handled differently than asynchronous communications. Bit duration in synchronous communications is not necessarily pre-defined at both the transmitting and receiving ends. Typically, in addition to the data signal, a clock signal is provided. This clock signal will mark the beginning of a bit cell on a pre-defined transmission. The source of the clock is predetermined and sometimes multiple clock signals are available. For example, if two nodes want to establish synchronous communications, point A could supply a clock to point B that would define all bit boundaries that A transmitted to B. Point B could also supply a clock to point A that would correspond to the data that A received from B. This example demonstrates how communications could take place between two nodes at completely different data rates. Character synchronization with synchronous communications is also very different than the asynchronous method of using start and stop bits to define the beginning and end of a character. When using synchronous communications a pre-defined character or sequence of characters is used to let the receiving end know when to start character assembly.

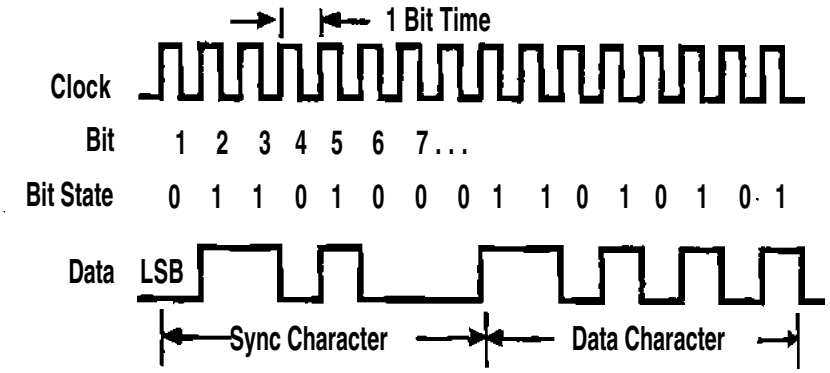

Figure 14: Synchronous Communications Bit Diagram

This pre-defined character is called a sync character or sync flag. Once the sync flag is received, the communications device will start character assembly. Sync characters are typically transmitted while the communications line is idle or immediately before a block of information is transmitted. To illustrate with an example, let's assume that we are communicating using eight bits per character. Point A is receiving a clock from point B and sampling the receive data pin on every upward clock transition. Once point A receives the pre-defined bit pattern (sync flag), the next eight bits are assembled into a valid character. The following eight bits are also assembled into a character. This will repeat until another pre-defined sequence of bits is received (either another sync flag or a bit combination that signals the end of the text, e.g., EOT). The actual sync flag and protocol varies depending on the sync format (SDLC, BISYNC, etc.).

For a detailed explanation of serial communications, please refer to the book *Technical Aspects of Data Communications* by John E. McNamara, published by Digital Press (DEC) 1982.

Appendix E: ACB Developer Toolkit Diskette and ACB Resource Kit

The ACB Developer Toolkit diskette provides sample software and technical insight to aid in the development of reliable applications and device drivers for the ACB family of communication cards. The goal in publishing this collection of source code and technical information is two-fold. First is to provide the developer with ample information to aid in the development of ACB based applications. Second is to provide a channel for suggestions back to our Technical Support Staff. The ACB Resource Kit provides a brief overview of the ACB product line and is available at your request. Topics concerning applications and integration are covered to provide a complete overview of the versatile ACB family. During ACB development, if any questions, comments, or suggestions arise, please contact Technical Support at the numbers listed at the end of this manual.

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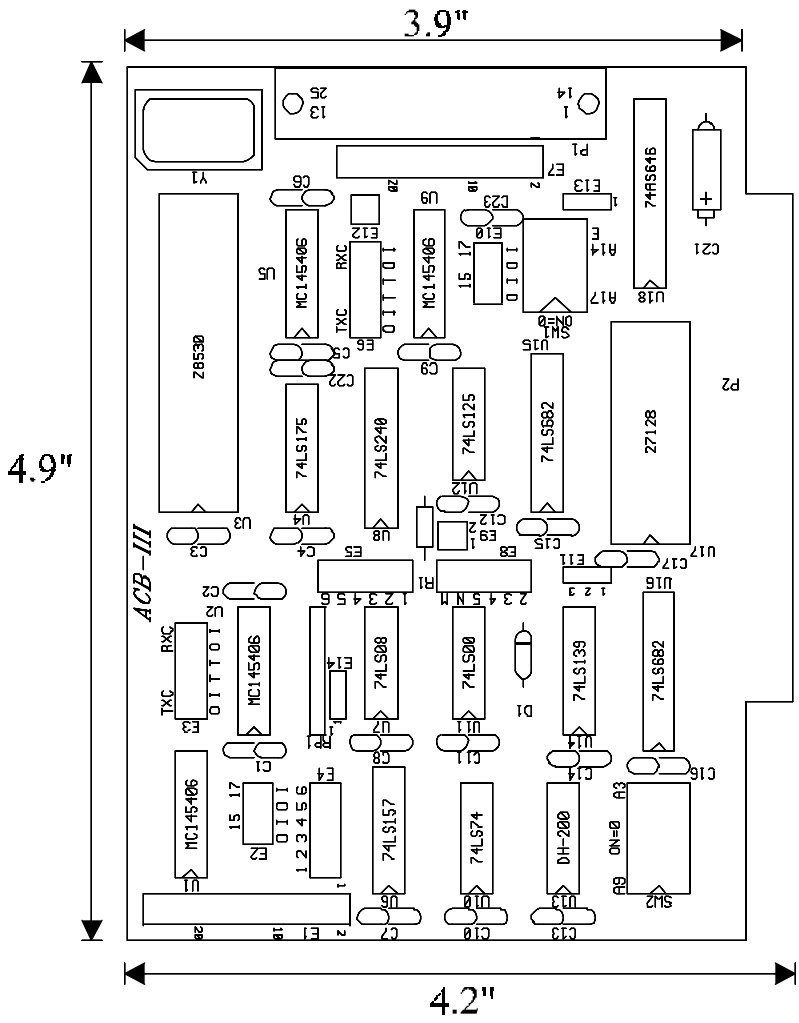
Appendix F: Silk-Screen



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August 28, 1997
San Diego, CA

Mr. Steven R. Peltier
President & Chief Executive Officer

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