INDUSTRIAL COMPUTER SOURCE®

Model ACB56
Product Manual

MANUAL NUMBER : 00750-002-3C

INDUSTRIAL COMPUTER SOURCE®

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FORWARD

This product manual provides information to install, operate and or program the referenced product(s) manufactured or distributed by Industrial Computer Source. The following pages contain information regarding the warranty and repair policies.

Technical assistance is available at: **1-800-480-0044**.

Manual Errors, Omissions and Bugs: A "Bug Sheet" is included as the last page of this manual. Please use the "Bug Sheet" if you experience any problems with the manual that requires correction.

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> To reduce risk of damage, returns of product must be in an Industrial Computer Source shipping container. If the original container has been lost or damaged, new shipping containers may be obtained from Industrial Computer Source Customer Service at a nominal cost.

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Current Revision 3C

August 1997

Chapter 1: Introduction

Overview

The Industrial Computer Source ACB56 provides the PC with one high speed RS-232 (V.24) or V.35 sync/async port and one RS-232 port suitable for use as a CSU command port. The ACB56 can be used in a variety of sophisticated communications applications such as SDLC, HDLC, X.25, and high speed async.

What's Included

The **ACB56** is shipped with the following items. If any of these items are missing or damaged, contact the supplier.

- **ACB56** Serial Interface Adapter
- 3.5" ACB Developers Toolkit Diskette
- User manual
- Warranty Extension Card

Factory Default Settings

The **ACB56** factory default settings are as follows:

Base Address	**DMA Channel**	**IRQ**	**Electrical Specification**
238	TX: 1/RX:3	5	V.35

To install the **ACB56** using factory default settings, refer to the section on Installation. For your reference, record installed **ACB56** settings below:

Base Address	**DMA Channel**	**IRQ**	**Electrical Specification**

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Chapter 2: Card Setup

The **ACB56** contains several jumper straps for each port which must be set for proper operation.

Address Selection

The **ACB56** occupies 8 consecutive I/O locations. A Dip-switch (SW1) is used to set the base address for these locations. Be careful when selecting the base address as some selections conflict with existing PC ports. The following table shows several examples that usually do not cause a conflict.

Address	Binary	Switch Settings						
	A9———A0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
238-23F	1000111XXX	Off	On	On	On	Off	Off	Off
280-287	1010000XXX	Off	On	Off	On	On	On	On
2A0-2A7	1010100XXX	Off	On	Off	On	Off	On	On
2E8-2EF	1011101XXX	Off	On	Off	Off	Off	On	Off
300-307	1100000XXX	Off	Off	On	On	On	On	On
328-32F	1100101XXX	Off	Off	On	On	Off	On	Off
3E8-3EF	1111101XXX	Off	Off	Off	Off	Off	On	Off

Figure 1: Address Selection Table

The following illustration shows the correlation between the Dip-switch setting and the address bits used to determine the base address. In the example below, the address 300 Hex through 307 Hex is selected. 300 Hex =11 0000 0XXX in binary representation.

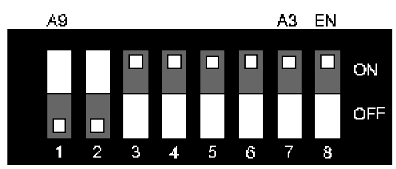


Figure 2: DIP-Switch Illustration

NOTE:

Setting the switch “On” or “Closed” corresponds to a “0” in the address, while leaving it “Off” or “Open” corresponds to a “1”.

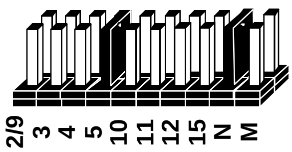
The relative I/O address of the 8530 SCC registers is as follows:

Base+0	Channel A Data Port
Base+1	Channel A Control Port
Base+2	Channel B Data Port
Base+3	Channel B Control Port
Base+4	Board Control/Status Port

Where "Base" is the selected board base address.

IRQ Selection (Header E6)

The **ACB56** has an interrupt selection jumper which should be set prior to use, if an interrupt is required by your application software. Consult the user manual for the application software being used to determine the proper setting. **E6** selects the interrupt request line (IRQ) for the ACB56. The diagram below shows IRQ 5 selected in a shared configuration. If no interrupt is desired, remove both jumpers.



2/9	Selects IRQ2/9
3	Selects IRQ3
4	Selects IRQ4
5	Selects IRQ5
10	Selects IRQ10
11	Selects IRQ11
12	Selects IRQ12
15	Selects IRQ15
N	Selects Normal (1 IRQ Per Board) IRQ Mode
M	Selects "Multi-IRQ" (Shared) IRQ Mode

Figure 3: Header E6, IRQ Selection (Shown in Factory Default)

NOTE:

The actual silk-screen for the **ACB56** may have a "2" in place of the IRQ "2/9" selection.

Interface Selection

RS-232

A DIP-shunt placed at E9 selects RS-232 (V.24).

V.35

A DIP-shunt placed at E10 selects V.35.

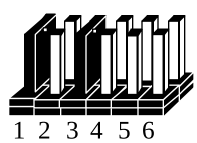
DMA Options

Headers E1 and E7 select the **D**irect **M**emory **A**ccess (DMA) mode of operation for the **ACB56**. Channel A of the SCC can operate in either half-duplex or full duplex DMA mode. Full duplex DMA can transmit and receive data simultaneously. Half-duplex DMA can transmit or receive data, but not in both directions simultaneously.

NOTE:

If DMA is not used, remove all of the jumpers on E1 and E7. Refer to Page 6 for the most common DMA settings.

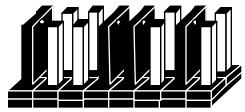
Header E1



1 DACK 1 Or 3 Acknowledge For Two Channel Mode
2 Two Channel A/B Mode A3B1
3 Two Channel A/B Mode A1B3
4 On = Ch. A Only / Off = Ch. B Only
5 DACK 3 DMA Acknowledge Channel 3
6 DACK 1 DMA Acknowledge Channel 1

Figure 4: Header E1 (Factory Default Settings)

Header E7



1 2 3 4 5 6 7 8

1 A or B Ch 3

2 A only Ch 3

3 A or B Ch 1

4 A only Ch 1

5 B Enable

6 A Full Duplex

7 DMA Tri-State drivers permanently enabled

8 DMA Tri-State drivers enabled by status / control port bit 7

Figure 5: Header E7 (Factory Default)

Positions 7 and 8 of Header E7 enable or disable DMA operation. A jumper "ON" position 7 permanently enables the DMA tri-state drivers. A jumper "ON" position 8 places DMA under software control via the DMA enable control port bit (located at Base+4). ***Removing the jumper disables the drivers, and no DMA can be performed.***

NOTE:

The power on reset signal disables the DMA enable signal. A jumper placed in position 7 of E7 will override any software use of the DMA enable/disable status port bit.

Commonly Used DMA Jumper Options

Option	E1	E7	Program 85230
No DMA	None	None	N/A

Single Channel DMA (Half-Duplex Only):

DMA Ch.1 Half Duplex	4,6	4	WAIT/REQ A
DMA Ch.3 Half Duplex.	4,5	2	WAIT/REQ A

Full Duplex using Both DMA Channels 1 and 3:

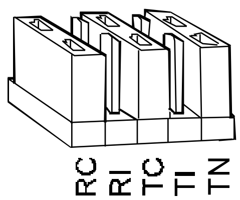
Ch.A DMA Ch.1 Receive Data				
Ch.A DMA Ch.3 Transmit Data	1,4	1,4,6	WAIT/REQ A	DTR/REQ A
Ch.A DMA Ch.3 Receive Data				
Ch.A DMA Ch.1 Transmit Data	1,4	2,3,6	WAIT/REQ A	DTR/REQ A

Figure 6: Commonly Used DMA Options

Remember that E7 positions 7 and 8 enable or disable DMA operation.

Header E5

Header E5 controls the clock input modes for the **ACB56**. The input clocks for the SCC can be set in either a non-inverted mode or in an inverted mode for application compatibility.



RC	Normal “non-inverted” Receive Clock Input (RTXC).
RI	Inverted Receive Clock Input.
TC	Normal “non-inverted” Transmit Clock Input (TRXC).
TI	Inverted Transmit Clock Input.
TN	Transmit Clock Input enable.

Figure 7: Header E5 (Factory Default)

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Chapter 3: Installation

The **ACB56** can be installed in any of the PC expansion slots, except J8 on the original IBM XT and Portable. The **ACB56** contains several jumper straps for each port which must be set for proper operation.

1. Turn off PC power. Disconnect the power cord.
2. Remove the PC case cover.
3. Locate an available slot and remove the blank metal slot cover.
4. Gently insert the **ACB56** into the slot. Make sure that the adapter is seated properly.
5. Replace the cover.
6. Connect the power cord.

Installation is complete.

Cabling Options

The **ACB56** has a number of cabling options available. These options include:

- **CAB/V35-36** - This cable provides a high quality shielded cable with the V.35 mechanical specification met on one end and a DB-25S (female) on the other end. V.35 has a mechanical specification that is impossible to place on a PC bracket and requires this adapter cable.
- **CA-104 -** This cable provides a 6' extension for use with RS-232 and V.35.

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Chapter 4: Technical Description

The **ACB56** utilizes the Zilog 85230 Serial Communications Controller (ESCC). This chip features programmable baud rate, data format and interrupt control, as well as DMA control. Refer to the Users Manual and the Zilog Datacom I/C Handbook for details on programming the SCC 85230 chip.

Features

- One channel of Sync/Async communications using 85230 .
- DMA supports data rate greater than 1 million bps (Bits Per Second)
- SCC channel B asynchronous port for CSU/DSU Command Port
- Selectable port address, IRQ level (2/9, 3, 4, 5, 10, 11, 12, 15), and DMA Channel (1 or 3)

Internal Baud Rate Generator

The baud rate of the SCC is programmed under software control. The standard oscillator supplied with the board is 7.3728 MHz. However, other oscillator values can be substituted to achieve different baud rates.

Programming The ACB56

Control/Status Port

The **ACB56** occupies eight **I**nput/**O**utput (I/O) addresses. The first four are used by the SCC chip, while the fifth address (Base+4) is the address of the on-board ***Control/Status Port.*** This port is used to set the **D**ata **T**erminal **R**eady (DTR) signal, to enable or disable DMA under program control, and to monitor the **D**ata **S**et **R**eady (DSR) input signals from the modem. The following table lists bit positions of the Control/Status port.

Bit	**Output Port Bits**		**Input Port Bits**	
0	DTR A	1=On, 0=Off	DSR A	1=On, 0=Off
1	DTR B	1=On, 0=Off	DSR B	1=On, 0=Off
2	Not Used	Not Used		
3	Not Used	Not Used		
4	Not Used	Not Used		
5	Not Used	Not Used		
6	Not Used	Not Used		
7	DMA Enable	1=On, 0=Off	Not Used	

Figure 8: Status/Control Register Bit Definitions

Software Examples

Function	Program Bits
Turn On CH.A DTR	Write Out Base+4,XXXX XXX1
Turn On CH.B DTR	Write Out Base+4,XXXX XX1X
Turn Off CH.A DTR	Write Out Base+4,XXXX XXX0
Turn Off CH.B DTR	Write Out Base+4,XXXX XX0X
Enable DMA Drivers	Write Out Base+4,1XXX XXXX
Disable DMA Drivers	Write Out Base+4,0XXX XXXX
Test CH.A DSR	Read In Base+4, Mask=0000 0001
Test CH.B DSR	Read In Base+4, Mask=0000 0010

Figure 9: Status Register Examples

Connector P3 Pin Assignments

RS-232 Signals

Signal	Name	Pin #	Mode
GND	Ground 7		
RD	Receive Data	3	Input RS-232
CTS	Clear To Send	5	Input RS-232
DSR	Data Set Ready	6	Input RS-232
DCD	Data Carrier. Detect	8	Output RS-232
TD	Transmit Data	2	Output RS-232
RTS	Request to Send	4	Output RS-232
TXC	Transmit Clock	15	Input/Output RS-232
RXC	Receive Clock	17	Input RS-232
TSET	Transmit Signal Element Timing	24	Output RS-232
DTR	Data Terminal Ready	20	Output RS-232

NOTE:

These assignments meet EIA/TIA/ANSI-232E DTE Specification.

V.35 Signals

Signal	Name	DB-25	V.35	Mode
GND	Ground	7	B	
RDB RX+	Receive Positive	16	T	Input
RDA RX-	Receive Negative	3	R	Input
TXCB TXC+	Transmit Clock Positive	12	AA	Input
TXCA TXC-	Transmit Clock Negative	15	Y	Input
RXCB RXC+	Receive Clock Positive	24	X	Input
RXCA RXC-	Receive Clock Negative	25	V	Input
TDB TX+	Transmit Positive	14	S	Output
TDA TX-	Transmit Negative	2	P	Output
TSETB TSET+	Transmit Signal Element Timing Positive	11	W	Output
TSETA TSET-	Transmit Signal Element Timing Negative	24	U	Output
CTS	Clear To Send	5	D	Input*
DSR	Data Set Ready	6	E	Input*
DCD	Data Carrier Detect	8	F	Input*
RI	Ring Indicator	22	J	Input*
DTR	Data Terminal Ready	20	H	Output*
RTS	Request To Send	4	C	Output*

NOTE:

All modem control signals are single ended (un-balanced) with RS-232 signal levels.

Connector P4 Pin Assignments

Signal	Name	Pin #	Mode
GND	Ground	5	
RD	Receive Data	2	Input RS-232
CTS	Clear To Send	8	Input RS-232
DSR	Data Set Ready	6	Input RS-232
DCD	Data Carrier Detect	1	Input RS-232
RI	Ring Indicator	9	Input RS-232
TD	Transmit Data	3	Output RS-232
RTS	Request To Send	7	Output RS-232
DTR	Data Terminal Ready	4	Output RS-232

These Pin Assignments meet the EIA/TIA/ANSI-574 DTE Specification

How to remain CE Compliant

In order for machines to remain CE compliant, only CE compliant parts may be used. To keep a chassis compliant it must contain only compliant cards, and for cards to remain compliant they must be used in compliant chassis. Any modifications made to the equipment may affect the CE compliance standards and should not be done unless approved in writing by Industrial Computer Source.

The Model ACB56 is designed to be CE Compliant when used in an CE compliant chassis. Maintaining CE Compliance also requires proper cabling and termination techniques. The user is advised to follow proper cabling techniques from sensor to interface to ensure a complete CE Compliant system. Industrial Computer Source does not offer engineering services for designing cabling or termination systems. Although Industrial Computer Source offers accessory cables and termination panels, it is the user's responsibility to ensure they are installed with proper shielding to maintain CE Compliance.

Chapter 5: Specifications

Environmental Specifications

Temperature Range

Operating

0º to 50º C (32º to 122º F)

Storage

-20º to 70º C (-4º to 158º F)

Humidity Range

10 to 90% R.H. Non-Condensing 10 to 90% R.H. Non-Condensing

Power Requirements

+5 VDC @ 410mA

+12 VDC @ 50mA

-12 VDC @ 50mA

Mean Time Between Failures (MTBF)

Greater than 150,000 hours. (Calculated)

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Appendix A: Troubleshooting

An ACB Developers Toolkit Diskette is supplied with the Industrial Computer Source adapter and will be used in the troubleshooting procedures. By using this diskette and following these simple steps, most common problems can be eliminated without the need to call Technical Support.

1. Identify all I/O adapters currently installed in your system. This includes your on-board serial ports, controller cards, sound cards etc. The I/O addresses used by these adapters, as well as the IRQ (if any) should be identified.
2. Configure your Industrial Computer Source adapter so that there is no conflict with currently installed adapters. No two adapters can occupy the same I/O address.
3. Make sure the Industrial Computer Source adapter is using a unique IRQ. While the Industrial Computer Source adapter does allow the sharing of IRQ's, many other adapters (i.e. SCSI adapters & on-board serial ports) do not. The IRQ is typically selected via an on-board header block. Refer to the section on Card Setup for help in choosing an I/O address and IRQ.
4. Make sure the Industrial Computer Source adapter is securely installed in a motherboard slot.
5. Use the supplied diskette and User Manual to verify that the Industrial Computer Source adapter is configured correctly. The supplied diskette contains a diagnostic program "SSDACB" that will verify if an adapter is configured properly. This diagnostic program is written with the user in mind and is easy to use. Refer to the "UTIL.txt" file found in the /UTIL sub-directory on the supplied diskette for detailed instructions on using "SSDACB".
6. The following are known I/O conflicts:

    - The 278 and 378 settings may conflict with your printer I/O adapter.
    - 3B0 cannot be used if a Monochrome adapter is installed.
    - 3F8-3FF is typically reserved for COM1:
    - 2F8-2FF is typically reserved for COM2:
    - 3E8-3EF is typically reserved for COM3:
    - 2E8-2EF is typically reserved for COM4:. This is a valid setup option for the **ACB56.** However, since only 10 address lines are actually decoded, a possible conflict with an advanced video card emulating the IBM XGA adapter (8514 register set) may occur.

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Appendix B: How To Get Assistance

Please refer to Appendix A - Troubleshooting prior to calling Technical Support.

1. Read this manual thoroughly before attempting to install the adapter in your system.
2. When calling for technical assistance, please have your user manual and current adapter settings. If possible, please have the adapter installed in a computer ready to run diagnostics.
3. Technical support is available Monday to Friday from 8:00 a.m. to 5:00 p.m. Pacific time. Technical support can be reached at (800) 480-0044.

RETURN AUTHORIZATION MUST BE OBTAINED FROM INDUSTRIAL COMPUTER SOURCE BEFORE RETURNED MERCHANDISE WILL BE ACCEPTED. AUTHORIZATION CAN BE OBTAINED BY CALLING INDUSTRIAL COMPUTER SOURCE AND REQUESTING A RETURN MERCHANDISE AUTHORIZATION (RMA) NUMBER.

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Appendix C: Electrical Interface

RS-232

Quite possibly the most widely used communication standard is RS-232. This implementation has been defined and revised several times and is often referred to as RS-232 or EIA/TIA-232. It is defined by the EIA as the *Interface between Data Terminal Equipment and Data Circuit- Terminating Equipment Employing Serial Binary Data Interchange*. The mechanical implementation of RS-232 is on a 25 pin D sub connector. The IBM PC computer defined the RS-232 port on a 9 pin D sub connector and subsequently the EIA/TIA approved this implementation as the EIA/TIA-574 standard. This standard is defined as the *9-Position Non-Synchronous Interface between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange.* Both implementations are in wide spread use and will be referred to as RS-232 in this document. RS-232 is capable of operating at data rates up to 20 Kbps at distances less than 50 ft. The absolute maximum data rate may vary due to line conditions and cable lengths. RS-232 often operates at 38.4 Kbps over very short distances. The voltage levels defined by RS-232 range from -12 to +12 volts. RS-232 is a single ended or unbalanced interface, meaning that a single electrical signal is compared to a common signal (ground) to determine binary logic states. A voltage of +12 volts (usually +3 to +10 volts) represents a binary 0 (space) and -12 volts (-3 to -10 volts) denotes a binary 1 (mark). The RS-232 and the EIA/TIA-574 specification defines two type of interface circuits, Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). The Industrial Computer Source adapter is a DTE interface.

V.35

V.35 is a standard defined by ITU (formerly CCITT) that specifies an electrical, mechanical, and physical interface that is used extensively by high-speed digital carriers such as AT&T Dataphone Digital Service (DDS). ITU V.35 is an international standard that is often refereed to as *Data Transmission at 48 Kbps Using 60 - 108 KHz Group-Band Circuits.* ITU V.35 electrical characteristics are a combination of unbalanced voltage and balanced current mode signals. Data and clock signals are balanced current mode circuits. These circuits typically have voltage levels from 0.5 Volts to -0.5 Volts (1 Volt differential). The modem control signals are unbalanced signals and are compatible with RS-232. The physical connector is a 34 pin connector that supports 24 data, clock and control signals. The physical connector is defined in the ISO-2593 standard. ITU V.35 specification defines two type of interface circuits, Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). The Industrial Computer Source adapter is a DTE interface.

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Appendix D: Direct Memory Access

In many instances it is necessary to transmit and receive data at greater rates than would be possible with simple port I/O. In order to provide a means for higher rate data transfers, a special function called **D**irect **M**emory **A**ccess (DMA) was built into the original IBM PC. The DMA function allows the **ACB56** (or any other DMA compatible interface) to read or write data to or from memory without using the Microprocessor. This function was originally controlled by the Intel 8237 DMA controller chip, but may now be a combined function of the peripheral support chip sets (i.e. Chips & Technology or Symphony chip sets).

During a DMA cycle the DMA controller chip is driving the system bus in place of the Microprocessor, providing address and control information. When an interface needs to use DMA it activates a DMA request signal (DRQ) to the DMA controller, which in turn sends a DMA hold request to the Microprocessor. When the Microprocessor receives the hold request it will respond with an acknowledge to the DMA controller chip. The DMA controller chip then becomes a Bus Master providing the necessary control signals to complete a Memory to I/O or I/O to Memory transfer. When the data transfer is started an acknowledge signal (DACK) is sent by the DMA controller chip to the **ACB56**. Once the data has been transferred to or from the **ACB56**, the DMA controller returns control to the Microprocessor.

To use DMA with the **ACB56** requires a thorough understanding of the PC DMA functions . The ACB Developers Toolkit demonstrates the setup and use of DMA with several source code and high level language demo programs. Please refer to the SCC User's Manual, the PC Technical Reference and the 8237 DMA controller chip specification for more information.

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Appendix E: Asynchronous and Synchronous Communications

Serial data communications implies that individual bits of a character are transmitted consecutively to a receiver that assembles the bits back into a character. Data rate, error checking, handshaking, and character framing (start/stop bits or sync characters) are pre-defined and must correspond at both the transmitting and receiving ends. The techniques used for serial communications can be divided two groups, *asynchronous* and *synchronous*.

When contrasting asynchronous and synchronous. serial communications, the fundamental differences deal with how each method defines the beginning and end of a character or group of characters. The method of determining the duration of each bit in the data stream is also an important difference between asynchronous and synchronous communications. The remainder of this section is devoted to detailing the differences between character framing and bit duration implemented in asynchronous and synchronous communications.

Asynchronous Communications

Asynchronous communications is the standard means of serial data communication for PC compatibles and PS/2 computers. The original PC was equipped with a communication or COM: port that was designed around an 8250 Universal Asynchronous Receiver Transmitter (UART). This device allows asynchronous serial data to be transferred through a simple and straightforward programming interface. Character boundaries for asynchronous communications are defined by a starting bit followed by a pre-defined number of data bits (5, 6, 7, or 8). The end of the character is defined by the transmission of a pre-defined number of stop bits (usual 1, 1.5 or 2). An extra bit used for error detection is often appended before the stop bits.

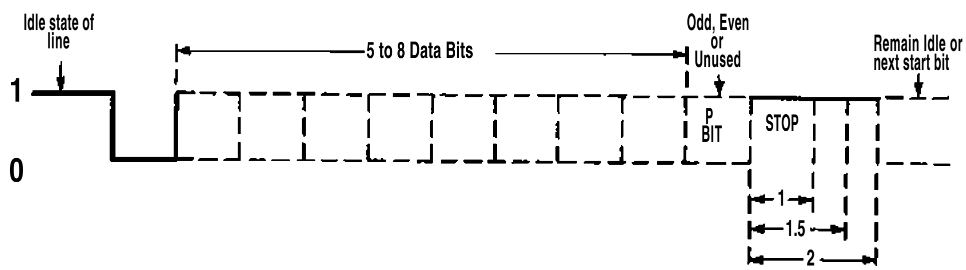

Figure 10: Asynchronous Communications Bit Diagram

This special bit is called the parity bit. Parity is a simple method of determining if a data bit has been lost or corrupted during transmission. There are several methods for implementing a parity check to guard against data corruption. Common methods are called (E)ven Parity or (O)dd Parity. Sometimes parity is not used to detect errors on the data stream. This is referred to as (N)o parity. Because each bit in asynchronous communications is sent consecutively, it is easy to generalize asynchronous communications by stating that each character is wrapped (framed) by pre-defined bits to mark the beginning and end of the serial transmission of the character. The data rate and communication parameters for asynchronous communications have to be the same at both the transmitting and receiving ends. The communication parameters are baud rate, parity, number of data bits per character, and stop bits (i.e. 9600,N,8,1).

Synchronous Communications

Synchronous Communications is used for applications that require higher data rates and greater error checking procedures. Character synchronization and bit duration are handled differently than asynchronous communications. Bit duration in synchronous communications is not necessarily pre-defined at both the transmitting and receiving ends. Typically, in addition to the data signal, a clock signal is provided. This clock signal will mark the beginning of a bit cell on a pre-defined transmission. The source of the clock is predetermined and sometimes multiple clock signals are available. For example, if two nodes want to establish synchronous communications, point A could supply a clock to point B that would define all bit boundaries that A transmitted to B. Point B could also supply a clock to point A that would correspond to the data that A received from B. This example demonstrates how communications could take place between two nodes at completely different data rates. Character synchronization with synchronous communications is also very different than the asynchronous method of using start and stop bits to define the beginning and end of a character. When using synchronous communications a pre-defined character or sequence of characters is used to let the receiving end know when to start character assembly.

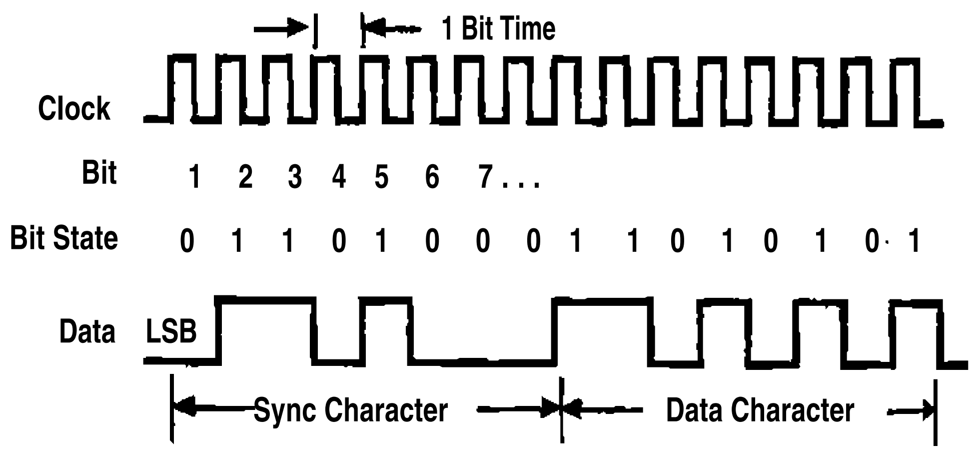

Figure 11: Synchronous Communications Bit Diagram

This pre-defined character is called a sync character or sync flag. Once the sync flag is received, the communications device will start character assembly. Sync characters are typically transmitted while the communications line is idle or immediately before a block of information is transmitted. To illustrate with an example, let's assume that we are communicating using eight bits per character. Point A is receiving a clock from point B and sampling the receive data pin on every upward clock transition. Once point A receives the pre-defined bit pattern (sync flag), the next eight bits are assembled into a valid character. The following eight bits are also assembled into a character. This will repeat until another pre-defined sequence of bits is received (either another sync flag or a bit combination that signals the end of the text, e.g., EOT). The actual sync flag and protocol varies depending on the sync format (SDLC, BISYNC, etc.).

For a detailed explanation of serial communications, please refer to the book *Technical Aspects of Data Communications* by John E. McNamara, published by Digital Press (DEC) 1982.

Appendix F: ACB Developer Toolkit Diskette and ACB Resource Kit

The ACB Developer Toolkit diskette provides sample software and technical insight to aid in the development of reliable applications and device drivers for the ACB family of communication cards. The goal in publishing this collection of source code and technical information is two fold. First is to provide the developer with ample information to develop ACB based applications. Second is to provide a channel for suggestions into the technical support efforts. The ACB Resource Kit provides a brief overview of the ACB product line and is available at your request. Topics concerning applications and integration are covered to provide a complete overview of the versatile ACB family. During ACB development, if any questions, comments, or suggestions arise, please contact Technical Support at the numbers listed at the front of this manual.

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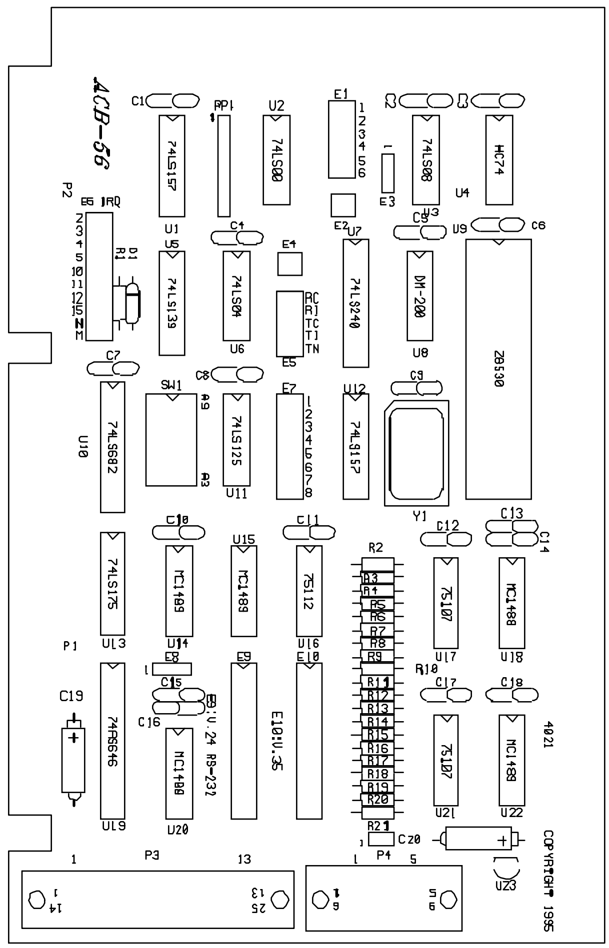
Appendix G: Silk-Screen



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August 28, 1997
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Mr. Steven R. Peltier
President & Chief Executive Officer

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