INDUSTRIAL COMPUTER SOURCE®

Model DIO48S/AT-P
Product Manual

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INDUSTRIAL COMPUTER SOURCE® http:/www.indcompsrc.com

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FOREWARD

This product manual provides information to install, operate and or program the referenced product(s) manufactured or distributed by Industrial Computer Source. The following pages contain information regarding the warranty and repair policies.

Technical assistance is available at: **1-800-480-0044**.

Manual Errors, Omissions and Bugs: A "Bug Sheet" is included as the last page of this manual. Please use the "Bug Sheet" if you experience any problems with the manual that requires correction.

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Chapter 1: Introduction

Features

- 48 Channels of Digital Input/Output.
- Interrupt Generation on Input Change of State.
- Change-of-state Interrupt Software Enabled in Six 8-Input Ports.
- All 48 I/O Lines Buffered on the Board.
- I/O Buffers Can Be Enabled/Disabled under Program Control.
- Four and Eight Bit Ports Independently Selectable for I/O.
- Hysteresis and Pull-Ups on I/O Lines.
- +5V Supply Available to the User.
- Compatible with Industry Standard I/O Racks like Gordos, Opto-22, Potter & Brumfield, etc.

Applications

- Automatic Test Systems.
- Laboratory Automation.
- Machine Control.
- Security Systems, Energy Management.
- Relay Monitoring and Control.
- Parallel Data Transfer to PC.
- Sensing Switch Closures or TTL, DTL, CMOS Logic.
- Driving Indicator Lights or Recorders.

A major feature of the DIO48S/AT-P is that the state of all inputs can be monitored and, if any state change occurs, a latched interrupt request can be generated. Thus, it is not necessary to use software to continuously poll the inputs to detect a change of state. The change-of-state interrupt is enabled by a software write to an interrupt-enable register. Six bits in that register each control an eight-input port at one of two type 8255-5 Programmable Peripheral Interface chips. The change-of-state interrupt latch can be cleared by a software write.

Also, bit C3 at each 24-bit port can be used as an external interrupt to the computer if jumpers are installed. When bit C3 goes high (edge triggering), an interrupt is requested. Interrupts from the ports are OR'ed together and OR'ed with the change-of-state interrupt. Interrupts are directed to levels #2 through #7, #10 through #12, #14 and #15.

The DIO48S/AT-P card was designed for industrial applications and can be installed in 7", or longer, I/O slots of IBM PC/XT/AT or compatible computers. Each I/O line is buffered and capable of sourcing 15 mA or sinking 24mA (64 mA or request). The card contains two Programmable Peripheral Interface chips type 8255-5 (PPI) to provide computer interface to 48 I/O lines. Each PPI provides three 8-bit ports A, B, and C. Each 8-bit port can be software configured to function as either inputs or output latches. Port C can also be configured as four inputs and four output latches.

Tristate I/O line buffers (74LS245) are configured automatically by hardware logic for input or output use according to direction assignment from a control register in the PPI. Further, if a jumper is properly placed on the card, the tristate buffers may be enabled/disabled under program control. (See the Option Selection chapter to follow.)

I/O wiring connections are via 50-pin headers on the board. Two flat I/O cables connect DIO48S/AT-P to termination panels such as Industrial Computer Source's model UTB-K. Also, this provides compatibility with Opto-22, Gordos, Potter & Brumfield, ect. module mounting racks. Every second conductor of the flat cables is grounded to minimize the effect of crosstalk between signals. If needed for external circuits, +5 VDC power is available on each I/O connector pin 49. If you use this power, we recommend that you include a 1A fast-blow fuse in your circuits in order to avoid possible damage to the host computer or cable in the event of a malfunction in those external circuits.

The DIO48S/AT-P occupies sixteen bytes of I/O address space. The base address is selectable via a DIP switch anywhere within the range of 000-3FF hex. Utility software provided on diskette with the DIO48S/AT-P card is a illustrated setup program. Interactive displays show locations and proper settings of DIP switches and jumpers to set up board address, interrupt levels, and interrupt enable.

Specifications

Digital Inputs

Logic High:	2.0 to 5.0 VDC.
Logic Low:	-0.5 to +0.8 VDC.
Input Load (Hi):	20 µA.
Input Load (Lo):	-200 µA.

Digital Outputs

Logic High:	2.5 VDC min., source 15 mA.
Logic Low:	0.5 VDC max., sink 24 mA.
	(64 mA optional)

Power Output

+5 VDC from computer bus (ext. 1A fast-blow fuse recommended).

Power Required

+5 VDC at 200 mA typical.

Size

7.15" Long.

Environmental

Operating Temperature:	0 to 60° C
Storage Temperature:	-50° to +120° C.
Humidity:	0 to 90% RH, non-condensing.

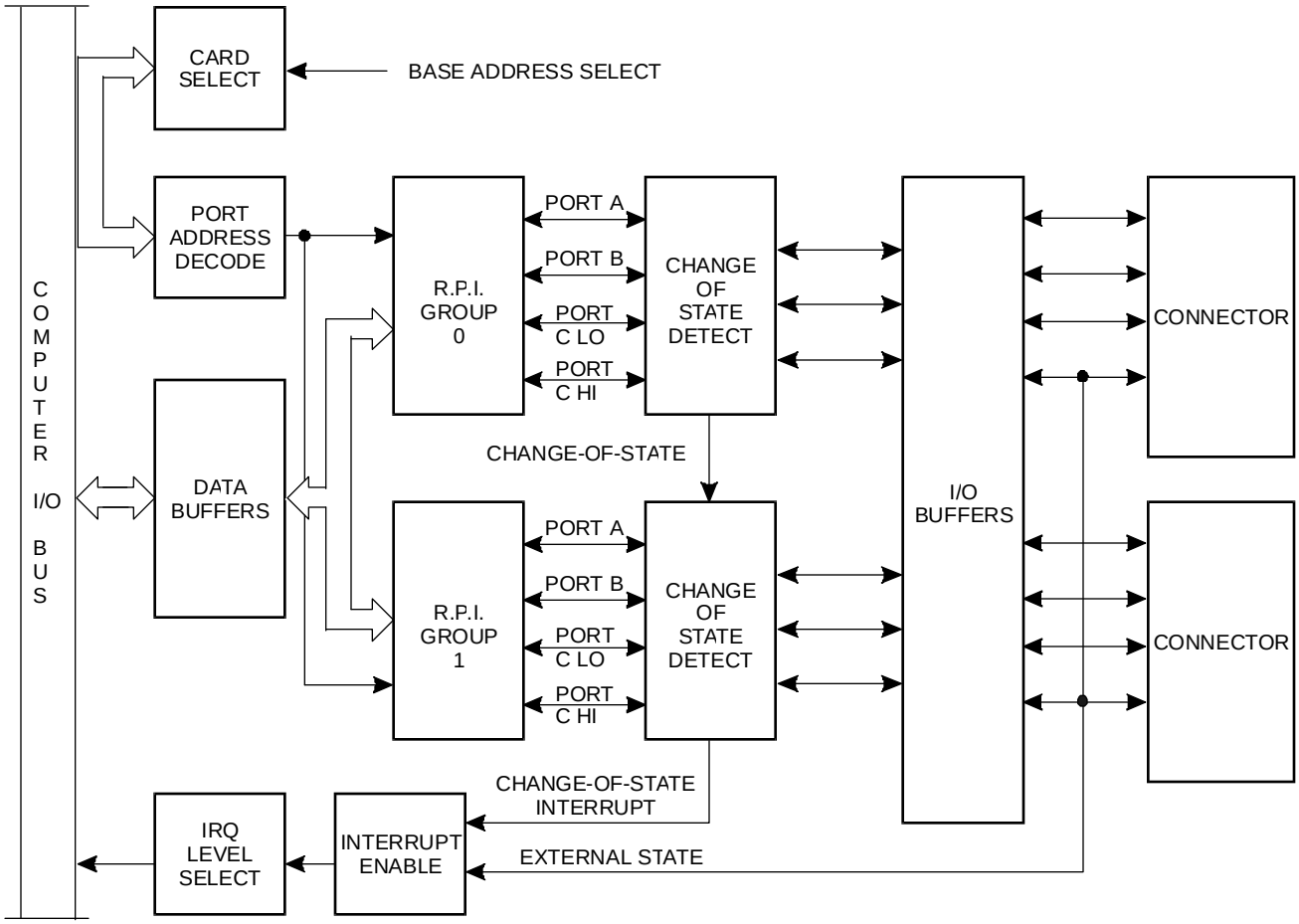

Figure 1-1: DIO48S/AT-P Block Diagram

How to remain CE Compliant

In order for machines to remain CE compliant, only CE compliant parts may be used. To keep a chassis compliant it must contain only compliant cards, and for cards to remain compliant they must be used in compliant chassis. Any modifications made to the equipment may affect the CE compliance standards and should not be done unless approved in writing by Industrial Computer Source.

The Model DIO48S/AT-P is designed to be CE Compliant when used in an CE compliant chassis. Maintaining CE Compliance also requires proper cabling and termination techniques. The user is advised to follow proper cabling techniques from sensor to interface to ensure a complete CE Compliant system. Industrial Computer Source does not offer engineering services for designing cabling or termination systems. Although Industrial Computer Source offers accessory cables and termination panels, it is the user's responsibility to ensure they are installed with proper shielding to maintain CE Compliance.

Chapter 2: Installation

The DIO48S/AT-P card can be installed in any slot of a PC/XT/AT compatible computer. Before installing the card, perform the software installation and run the setup program, **DIO48SET.EXE.** Also, read the OPTION SELECTION and ADDRESS SELECTION chapters of this manual and configure the card according to your requirements. Be especially careful with address selection. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior. Included on your Master Disk is a routine called **FINDBASE.EXE.** After installing the software, run this program to help in finding the proper address space for the card. **FINDBASE.EXE** is described further on in this chapter.

Software Installation

Installation Program

The software should be installed prior to card installation into the chassis. A setup routine titled **DIO48SET.EXE** describes how to set all the address switches and jumpers on the card. Each of the settings is also described in its appropriate section of this manual.

This package uses compression to simplify installation and to permit use of a single diskette. A program is provided on your master disk to copy and expand the software package onto your hard drive. To begin installation, place the software master disk into a floppy drive and execute the **INSTALL.EXE** program.

For example, if you have placed the master disk in floppy drive A, you would type `" A:INSTALL [ENTER] "` to execute the installation program.

The installation program will ask you for various installation options, and will provide default settings. The default settings may be selected (by pressing ENTER 0 if they work for your particular system setup, or you can respond to the questions with appropriate answers as needed.

When all the installation options have been set, the program will expand the program files onto the destinations you have selected. Once this process is complete, please put your Master Disk in a safe place as a backup.

Findbase Routine

One of the programs included in the installation is a routine titled **FINDBASE.EXE**. This program can be used to find an unused section of I/O memory to assign to the DIO48S/AT-P. It simplifies base address selection. The program will scan your computer's I/O ports for available locations which would be suitable for the card. The program asks you to pick the number of address bytes required from the supplied list. In this case, the DIO48S/AT-P requires 16 address bytes so select 16 from the list. It will then present the first address location with that much space available. The instructions are self explanatory. A text file, **FINDBASE.TXT** contains more information on its use.

Hardware Installation

Before installing the card, be sure to install the software as described above, and run the **DIO48SET.EXE** program. Check the appropriate sections of this manual for further information on address and option selections.

To install the card:

1. Perform the Software Installation described above.
2. Turn off computer power.
3. Remove the computer cover.
4. Remove the blank I/O backplate.
5. Set the Interrupt option jumpers as desired. See setup program provided on the diskette provided with this card and OPTION SELECTION, chapter 3 of this manual.
6. Set the base address. See Setup program provided on the diskette provided with this card and ADDRESS SELECTION, chapter 4 of this manual.
7. Feed the flat I/O interface cables through the opening in the backplate.
8. Plug in the I/O interface cables to the headers on the DIO48S/AT-P card.
9. Install the card in an I/O expansion slot.
10. Inspect for proper fit of the card and cables, and tighten screws.
11. Replace the computer cover and apply power.

Chapter 3: Option Selection

Refer to the setup programs on the diskette provided with the card. Also, refer to Figure 1-1: DIO48S/AT-P: Block Diagram, and Figure 3-1: Option Selection Map on the following page when reading this chapter of the manual.

External Interrupts are accepted on the I/O connector pin 9 (bit C3). The Interrupt signal is positive true. External Interrupts are enabled if the IEN jumper is installed. A separate IEN jumper, IEN0 and IEN1, is provided for each 8255 section. Interrupts are directed to levels #3 through #7, #10 through #12, #14 and #15 by jumpers installed at locations labelled IRQ2 through IRQ7, IRQ10 through IRQ12, IRQ14 and IRQ15 respectively.

A means of enabling or disabling the 74LS245 input/output buffers under program control is provided at the jumper position labelled TST/BEN. When the jumper is in the BEN (Board Enable) position, the I/O buffers are always enabled. When the jumper is in the TST (Tristate) position, enabled/disabled state is controlled by a control register. (See the programming chapter of this manual for a description.)

Note: A jumper must be installed in either the TST or the BEN position for the card to function.

An LED, CR1, is provided on the top of the board to offer assistance in program development. Each time an interrupt is generated, the LED will be lit and latched ON until the interrupt is RESET. If there is an immediate RESET of the interrupt, however, it is likely that the LED will not remain lit long enough to be observed

The foregoing are the only manual setups necessary to use the DIO48S/AT-P. Input/Output selection and the change-of-state Interrupt Enable is done via software by writing to a control register in each PPI as described in the PROGRAMMING chapter of this manual.

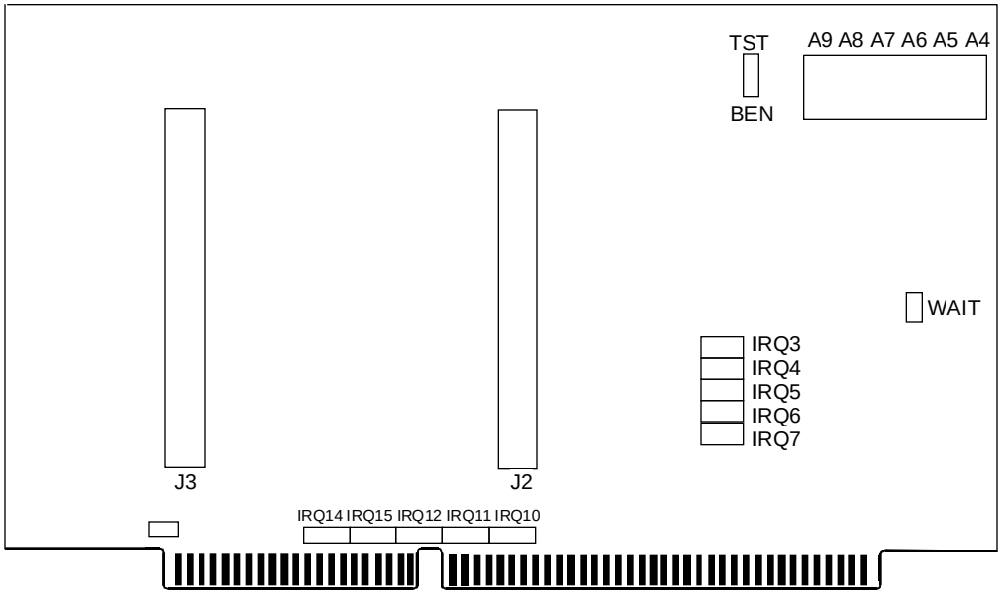

Figure 3-1: DIO48S/AT-P Option Selection Map

Chapter 4: Address Selection

The DIO48S/AT-P card occupies 16 bytes of I/O space. The card base address can be selected anywhere within the I/O address range 000-3FF hex. However two installed options cannot share the same address. If you are certain of your available disk space, run the FINDBASE utility provided on the included diskette. Refere to the Findbase section of Chapter 2 for further information.

Hex Range	Usage
000-1FF	Internal System - Not Usable
200-20F	Game Control
210-217	Expansion Unit
220-24F	Reserved
278-27F	Reserved
2E8-2EF	Serial Port
2F0-2F7	Reserved
300-31F	Asynchronous Communications (secondary)
320-32F	Prototype Card
378-37F	Fixed Disk
380-38C	Printer
3A0-3A9	SDLC Communications
3B0-3BF	Binary Synchronous Communications (primary)
3C0-3CF	Reserved
3DO-3DF	Color/Graphics
3E0-3E7	Reserved
3E8-3EF	Serial Port
3F0-3F7	Diskette
3F8-3FF	Asynchronous Comunications (primary)

Table 4-1: Standard Base Address Table

To set desired board address, refer to the illustrated Board Address setup program on the Utility deskette provided with the card. Type the desired address in hexadecimal code and the graphic display shows you how to set the ADDRESS SETUP switches. These switches are marked A4-A9 and form a binary representation of the address in negative-true logic. **(Assign '0' to all ADDRESS SETUP switches turned ON, and assign '1' to all ADDRESS SETUP switches turned OFF)**.

Switch Label	A9	A8	A7	A6	A5	A4	A3
Address Line Controlled	A9	A8	A7	A6	A5	A4	A3

The following example illustrates switch selection corresponding to hex 2D0 (or binary 10 1101 xxxx). The "xxxx" represents address lines A3, A2, A1, and A0 used on the Card to select individual registers at the PPI's. See Chapter 5, Programming.

Hex Representation	2 + 0 = 2		8 + 4 + 0 + 1 = 13 = D (hex)			
Conversion Multipliers	2	1	8	4	2	1
Binary Representation	1	0	1	1	0	1
Setup	OFF	ON	OFF	OFF	ON	OFF
Switch ID. (label)	A9	A8	A7	A6	A5	A4

Note: Carefully review the address selection reference table on the previous page before selecting the card address. If the addresses of two installed functions overlap you will experience unpredictable computer behavior.

Chapter 5: Programming

Industrial Computer Source supplies three programs to support the DIO48S/AT-P Digital I/O card and, also, to help you develop your applications software. These programs are on a diskette that comes with your card and are as follows:

DIO48SET.EXE This is a menu-driven, pictorial program to help you set the card address level, change-of-state interrupt, and high level interrupt enable.

SAMPLE1.C C-language software modules defining function prototypes, direct software interface, and a root module to demonstrate change-of-state programming.

DEMO.EXE A demonstration program.

A total of 16 address locations are used by the DIO48S/AT-P. The PPI's are addressed consecutively with Address bits A3 through A0 as follows:

Address	Port Assignments	Operation
Base Address + 0	PA port 0	Read/Write
Base Address + 1	PB port 0	Read/Write
Base Address + 2	PC port 0	Read/Write
Base Address + 3	Control Port 0	Write Only
Base Address + 4	PA port 1	Read/Write
Base Address + 5	PB port 1	Read/Write
Base Address + 6	PC port 1	Read/Write
Base Address + 7	Control Port 1	Write Only
Base Address + B	Enable chg-of-st. Int	Write Only
Base Address + F	Clr chg-of-st. Int	Write Only

Table 5-1: DIO48S/AT-P Address Selection

The DIO48S/AT-P card uses two 8255-5 PPI's to provide a total of 48 bits input/output capability. The card is designed to use each of these PPI's in Mode 0 wherein:

a. There are two 8-bit ports (A and B) and two 4-bit ports (C Hi and C Lo).
b. Any port can be configured as an input or an output.
c. Outputs are latched.
d. Inputs are not latched.

Each PPI contains a control register. This write-only, 8-bit register is used to set the mode and direction of the ports. At Power-Up or Reset, all I/O lines are set as inputs. Each PPI should be configured during initialization by writing to the control registers even if the ports are only going to be used as inputs. Output buffers are automatically set by hardware according to the control register states. Note that control registers are located at base address +3 and base address +7. Bit assignments in each of these control registers are as follows:

D0 - Port C Lo (C0-C3)	1 - Input	0 - Output
D1 - Port B	1 - Input	0 - Output
D2 - Mode Selection	1 - Mode 1	0 - Mode 0
D3 - Port C Hi (C4 - C7)	1 - Input	0 - Output
D4 - Port A	1 - Input	0 - Output
D5, D6 - Mode Selection	01 - Mode 1	00 - Mode 0, 1X - Mode 2
D7 - Mode Set Flag	1 - Active	

Table 5-2: Control Register Bit Assignments

NOTE:

Mode 1 and Mode 2 cannot be used by the DIO48S/AT-P. Thus, bits D2, D5, and D6 should always be set to "0" and bit D7 to "1".

At Power-Up or Reset, the change-of-state interrupt-enable register is set to zero. This enables all inputs to generate change-of-state interrupts. During initialization this register should be programmed to prevent interrupt generation by ports programmed as outputs or by inputs that you do not want to cause change-of-state interrupts. In order to program the change-of-state interrupt-enable register, write to it at base address +B. Data bits D0 through D5 are used to enable inputs corresponding to ports A, B, and C of the 8255 PPI's. Writing a "one" disables the port; writing a "zero" enables it.

Bit	Port Controlled
D0	Group 0, Port A
D1	Group 0, Port B
D2	Group 0, Port C
D3	Group 1, Port A
D4	Group 1, Port B
D5	Group 1, Port C

Table 5-3: Change-of-State Interrupt Enable Register

The change-of-state Interrupt is latched. To clear this latch, write anything at location (Base Address +F).

Enabling/Disabling I/O Buffers

DIO48S/AT-P provides a means for enabling/disabling the tristate I/O buffers under program control. If the TST/BEN jumper on the card is installed in the BEN position, the I/O buffers are permanently enabled. However, if that jumper is in the TST position, the buffers are software controlled via the control register as follows:

a. The card is initialized in the receive (input) mode by the computer reset command.

b. When bit D7 of the control register is set high, direction of the three ports of the associated PPI chip can be set. For example, a write to base address +3 with data bit D7 high allows programming of port direction at Group 0 ports A, B, the Group 0 PPI will be configured in mode 0 with Ports A, B, and C as outputs.

c. Now, if any of the ports have been set as outputs, you may set the initial values to the respective port with the outputs still in the tristate condition. (If all ports have been set as inputs, this step is not necessary.)

d. If data bit D7 is low when the control byte is written, ONLY the associated buffer controller is addressed. If, for example, a control byte of hex 80 has been sent as previously described, and the data to be output are correct, and it is now desired to open the three ports, then it is necessary to send a control byte of hex 00 to base address +3 to enable the Group 0 buffers. When you do this, the buffers will be enabled.

Note: Note that all data bits except D7 must be the same for the two control bytes.

Those buffers will now remain enabled until another control byte with data bit D7 high is sent to base address +3.

Similarly, the Group 1 ports can be enabled/disabled via the control register at base address +7. The following program fragment in C language illustrates the foregoing:

```
const BASE_ADDRESS 0x300;

outportb(BASE_ADDRESS +3, 0x89);    /*This instruction sets the mode to Mode 0,
                                    ports A and B as output, and port C as
                                    input.  Since bit D7 is high, the output
                                    buffers are set to tristate condition.  See
                                    item b. above.*/

outportb(BASE_ADDRESS,0);

outportb(BASE_ADDRESS+1,0);         /*These instructions set the initial state
                                    of ports A and B to all zeroes.  Port C is
                                    not set because it is configured as an in-
                                    put. See item c. above.*/

outportb(BASE_ADDRESS +3, 0x09);    /*Enable the tristate output buffers by using
                                    the same control byte used to configure the
                                    PPI, but now set bit D7 low.  See item d.
                                    above.*/
```

Using Visual Basic

Included with the supplied software is a DLL (Dynamic Link Library) called **VBACCES.DLL.** It is compatible with Visual Basic version 3.0. **VBACCES.DLL** must be copied to your Windows directory. Also included is a sample program to help you interface this DLL with Visual Basic. The program is titled **VBACCES.FRM**, and its global definition file is **VBACCES.GBL**. The information in the **.GBL** file must be contained in any application that uses the DLL, but does not have to be in a separate file. A project file **VBACCES.MAK** is also included.

The commands provided are:

OutPort, Outportb:	Allows write access to the I/O bus, similar to the C language outport and outportb functions.
InPort, InPortb:	Allows read access to the I/O bus, similar to the C language inport and inportb functions.
Peek, Poke:	Allows read and write access to RAM, similar to BASIC's Peek and Poke statements.

Please refere to the **VBACCES.GBL** file for programming information related to the above function.

Chapter 6: Connector Pin Assignments

Two 50-pin headers are provided on the DIO48S/AT-P; one for each 24 I/O group. The mating connector is an AMP type 1-499776-0 or equivalent. Connector pin assignments are listed below. Notice that every second line is grounded to minimize crosstalk between signals.

Assignment		Pin	Pin	Assignment
Port C High	PC7	1	2	Ground
Port C High	PC6	3	4	Ground
Port C High	PC5	5	6	Ground
Port C High	PC4	7	8	Ground
Port C Low	PC3*	9	10	Ground
Port C Low	PC2	11	12	Ground
Port C Low	PC1	13	14	Ground
Port C Low	PC0	15	16	Ground
Port B	PB7	17	18	Ground
Port B	PB6	19	20	Ground
Port B	PB5	21	22	Ground
Port B	PB4	23	24	Ground
Port B	PB3	25	26	Ground
Port B	PB2	27	28	Ground
Port B	PB1	29	30	Ground
Port B	PB0	31	32	Ground

(continued on next page)

Assignment		Pin	Pin	Assignment
Port A	PA7	33	34	Ground
Port A	PA6	35	36	Ground
Port A	PA5	37	38	Ground
Port A	PA4	39	40	Ground
Port A	PA3	41	42	Ground
Port A	PA2	43	44	Ground
Port A	PA1	45	46	Ground
Port A	PA0	47	48	Ground
+5VDC		49	50	Ground

Appendix A: 8255 Data Sheet

The data sheets in this Appendix are provided to help your understanding of the 8255-5 PPI which is made by a number of companies.

The information, diagrams, and all other data included are believed to be correct and reliable. However, no responsibility is assumed by Mitsubishi Electric Corporation for their use, nor for any infringements of patents or other rights belonging to third parties which may result from their use. Values shown on these data sheets are subject to change for product improvement.

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Declaration of Conformity

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Industrial Computer Source declares under its own and full responsibility that the following products are compliant with the protection requirements of the 89/336/EEC and 73/23/EEC directives.

Only specific models listed on this declaration and labeled with the CE logo are CE compliant.

DIO48S/AT-P

Conformity is accomplished by meeting the requirements of the following European harmonized standards:

EN 50081-1:1992 Emissions, Generic Requirements.

-EN 55022 Measurement of radio interference characteristics of information technology equipment.

EN 50082-1:1992 Immunity, Generic Requirements.

-IEC 801-2:1984 Immunity for AC lines, transients, common, and differential mode.
-IEC 801-3:1984 Immunity for radiated electromagnetic fields.
-IEC 801-4:1988 Immunity for AC and I/O lines, fast transient common mode.

EN 60950:1992 Safety of Information Technology Equipment.

Information supporting this declaration is contained in the applicable Technical Construction file available from:

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August 29, 1997
San Diego, CA

Mr. Steven R. Peltier
President & Chief Executive Officer

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San Diego, CA 92121-0557

Your Name: _____

Company Name: _____

Address 1: _____

Address 2: _____

Mail Stop: _____

City: _____ State: _____ Zip: _____

Phone: (_____) _____

Product: **DIO48S/AT-P**

Manual Revision: **00650-096-35B**

Please list the page numbers and errors found. Thank you!