Model AOB6-P
Product Manual

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6260 SEQUENCE DRIVE, SAN DIEGO, CA 92121-4371 (619) 677-0877 (FAX) 619-677-0895

INDUSTRIAL COMPUTER SOURCE EUROPE *TEL (1) 69.18.74.40 FAX (1) 64.46.40.42* • ***INDUSTRIAL COMPUTER SOURCE (UK) LTD*** *TEL 01243-533900 FAX 01243-532949*

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Chapter 1: Functional Description

The AOB6-P is a full-size card that can be installed in long slots of PC/XT/AT class computers. It contains six digital-to-analog converters (DAC) and twenty-four programmable digital I/O channels. Each analog output channel can be independently configured for voltage ranges of:

0V to +5V,
0V to +10V,
-2.5V to +2.5V,
-5V to +5V,
-10V to +10V

or for current ranges of:

1mA to 5mA,
4mA to 20mA.

With the addition of one resistor per channel the analog outputs can also be configured for a current range of:

0mA to 50mA,

All analog output channels have double-buffered inputs for single-step update and each is addressed at its own I/O location. Analog output channels can be user-selected to provide simultaneous updating by either software or external signal. That updating is user-assignable in pairs of channels or all DAC channels can be updated simultaneously.

Digital I/O channels are provided from a type 8255 Programmable Peripheral Interface chip (PPI). The 8255 PPI is a general purpose programmable I/O device. It provides 24 bits of digital I/O and may be programmed for three major modes of operation.

In MODE 0 each group of 24 I/O pins may be programmed to be input or output. That programming can be in sets of eight for ports A and B and in sets of four for port C. In MODE 1, each group may be programmed to have eight lines of input or output. Of the remaining four pins, three are used for handshaking and interrupt control signals. In MODE 2, eight lines are used for bi-directional bus and five lines are used for handshaking. A detailed description of the 8255 PPI is contained in Appendix C.

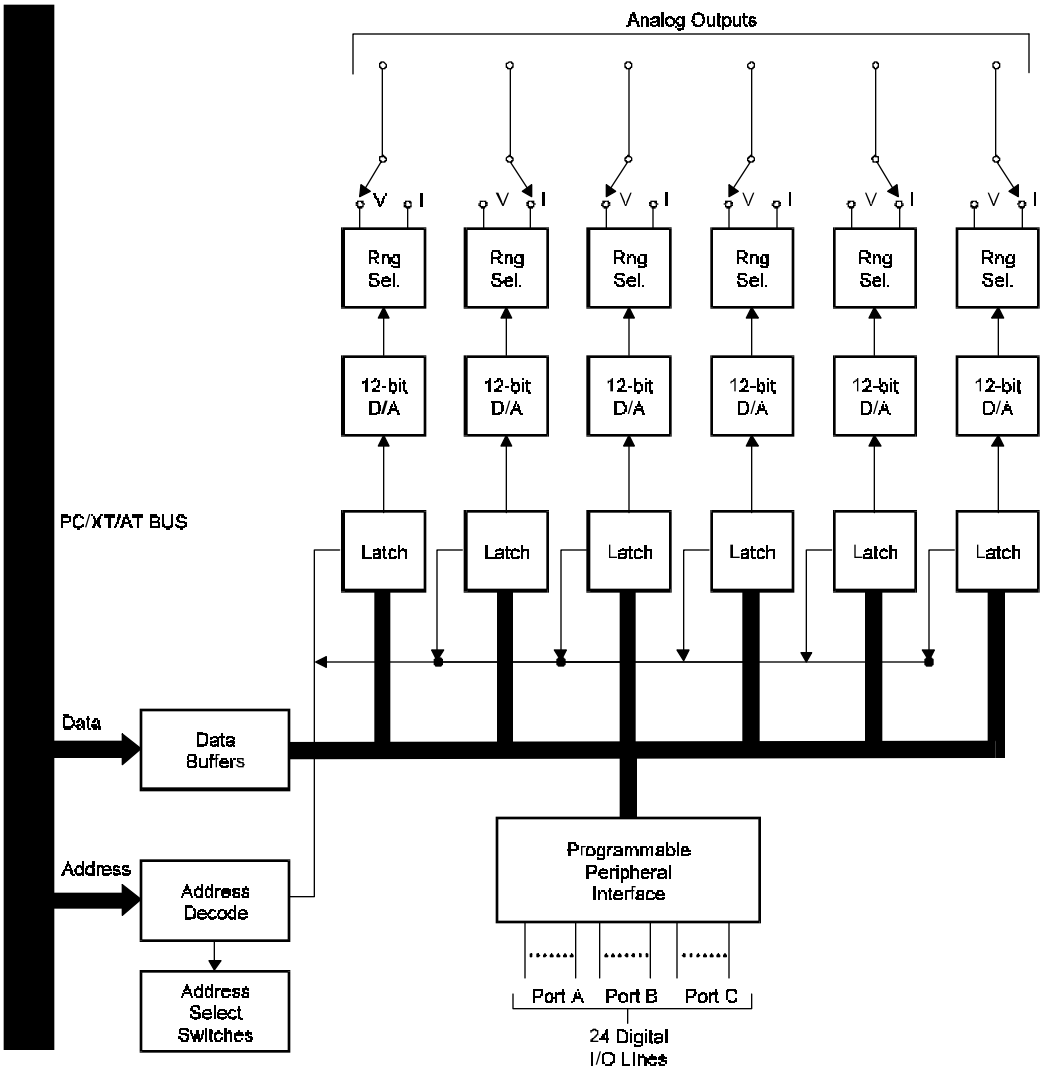

Figure 1-1: AOB6-P Card - Block Diagram

How to remain CE Compliant

In order for machines to remain CE compliant, only CE compliant parts may be used. To keep a chassis compliant it must contain only compliant cards, and for cards to remain compliant they must be used in compliant chassis. Any modifications made to the equipment may affect the CE compliance standards and should not be done unless approved in writing by Industrial Computer Source.

The Model AOB6-P is designed to be CE Compliant when used in an CE compliant chassis. Maintaining CE Compliance also requires proper cabling and termination techniques. The user is advised to follow proper cabling techniques from sensor to interface to ensure a complete CE Compliant system. Industrial Computer Source does not offer engineering services for designing cabling or termination systems. Although Industrial Computer Source offers accessory cables and termination panels, it is the user's responsibility to ensure they are installed with proper shielding to maintain CE Compliance.

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Chapter 2: Installation

Address Seleciton

Refer to Item 1, “Set Board Address” on the AOB6-P Board Setup and Calibration diskette provided by I.C.S. The card requires 16 consecutive address locations in I/O space. The starting, or base, address can be selected anywhere within the I/O address range 000-3FF hex, providing that the address does not overlap with other functions. If in doubt, refer to the Table below for a list of standard address assignments.

Hex Range	Usage
000-00F	DMA Chip 8237A-5
020-021	Interrupt 8259A
040-043	Timer 8253-5
060-063	PPI 8255A-5
080-083	DMA Page Register
0AX	NMI Mask Register
0CX	Reserved
0EX	Reserved
100-1FF	Not Usable
200-20F	Game Control
210-217	Expansion Unit
220-24F	Reserved
278-27F	Reserved
2F0-2F7	Reserved
2F8-2FF	Asynchronous Communication (secondary)
300-31F	Prototype Card
320-32F	Fixed Disk
378-37F	Printer
380-38C **	SDLC Communications
380-389 **	Binary Synchronous Comm. (secondary)
3A0-3A9	Binary Synchronous Comm. (primary)
3B0-3BF	IBM Monochrome Display/Printer
3C0-3CF	Reserved
3D0-3DF	Color/Graphics
3E0-3E7	Reserved
3F0-3F7	Diskette
3F8-3FF	Asynchronous Communication (primary)

** These options can not be used together - addresses overlap

Table 2-1: IBM Memory Map

The base address is set by a DIP switch which controls address bits A4 through A9.

In order to select the base address, convert the desired address to binary. Then for each "1" of the binary address, set the corresponding DIP switch to OFF, and for each "0" of the binary address set the corresponding switch to ON.

For example, to program a base address of hex 300, DIP switches A9 and A8 are set to the "OFF" position, while switches A7 through A4 are set to the "ON" position.

The following example illustrates this process in detail: In this case, switch selection corresponds to binary 10 1101 xxxx (or hex 2D0). The "xxxx" represents address lines A3, A2, A1, and A0 used on the card to select individual registers. See Chapter 3, PROGRAMMING.

Address Line Controlled	A9	A8	A7	A6	A5	A4
Switch Label	A9	A8	A7	A6	A5	A4
Setup	OFF	ON	OFF	OFF	ON	OFF
Binary representation	1	0	1	1	0	1
Conversion factors	2	1	8	4	2	1
Hex representation	2D					

Table 2-2: Example of Address Selection

Review the Address Selection Reference Table carefully before selecting card address. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior.

Option Selection

Refer to the Block Diagram and Option Selection Map when reading this section. Card operation is determined by jumper installation and switch settings as described in the following paragraphs.

Analog Output, Mode, Voltage or Current

Each analog output channel can be configured as a voltage or current output by installation of jumpers in locations marked V0 through V5, or I0 through I5.

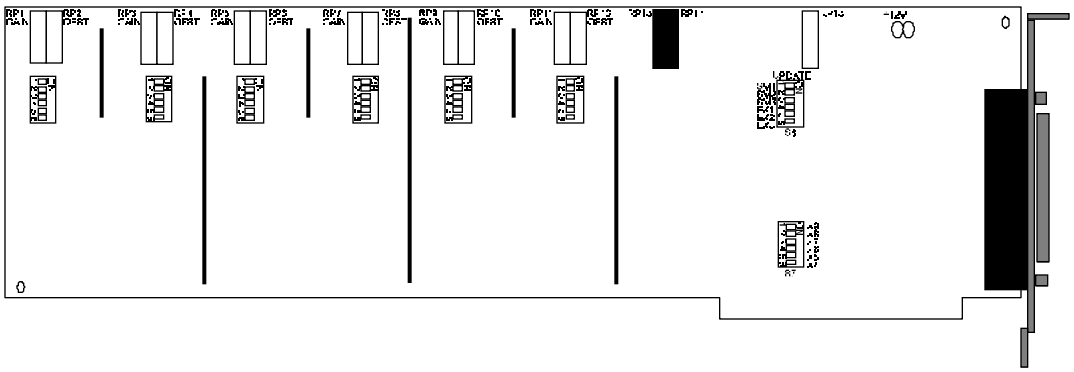


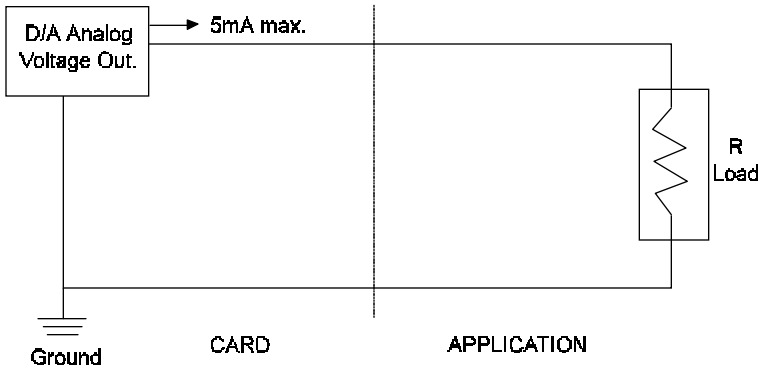
Figure 2-1: AOB6-P Card- Option Selection Map

Output Ranges

The output ranges are individually selected for each analog output channel 0 through 5 individually by corresponding switches S0 through S5. The following tables list switch settings for the desired output range.

Analog Output		**Switch Position**				
Voltage Range (jmp.V in)	**1**	**2**	**3**	**4**	**5**	**6**
0V to 5V	ON	OFF	OFF	OFF	ON	OFF
0V to 10V	OFF	ON	OFF	OFF	ON	OFF
2.5V to +2.5V	ON	OFF	OFF	ON	ON	OFF
-5V to +5V	ON	OFF	OFF	ON	OFF	OFF
-10V to +10V	OFF	ON	OFF	ON	OFF	OFF

Table 2-3: Selecting Voltage Range

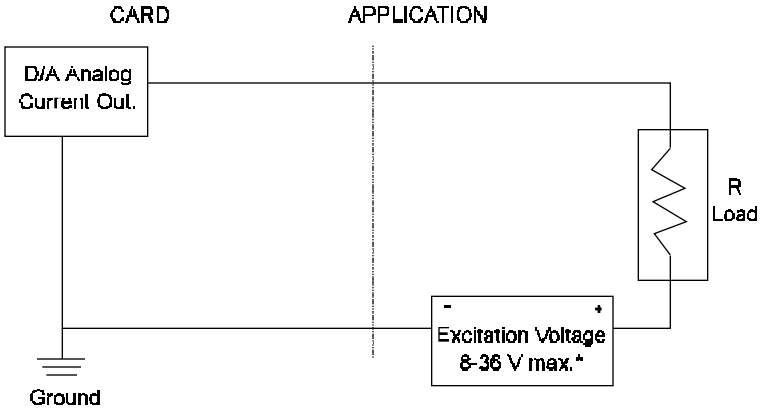


Analog Output		**Switch Position**				
Current Range (jmp.I in)	**1**	**2**	**3**	**4**	**5**	**6**
1 - 5 mA	ON	OFF	ON	OFF	ON	OFF
4 - 20 mA	ON	OFF	ON	OFF	ON	ON
0 - 50 mA *	ON	OFF	OFF	OFF	ON	ON

* Signifies option requiring addition of one 167 ohm resistor per channel.

Table 2-4: Selecting Current Range

Add R7a for channel AO0;
Add R37a for channel AO3
Add R17a for channel AO1;
Add R47a for channel AO4
Add R27a for channel AO2;
Add R57a for channel AO5



* Excitation Voltage up to 60V is OK on low current ranges. Minimum voltage of 8V must be maintained for correct operation.

CAUTION

Do not connect current loops to a DAC that is set to voltage mode. The loop supply can cause irreversible damage to the DAC.

Analog Output Update Mode

The analog-output update mode is selected by six-position DIP switch S6. Labels printed alongside the switch facilitate selection. Switches are enabled when placed in the ON position.

Three analog-output update modes are available: (a) Individual update of each channel upon high-byte Write, (b) Simultaneous update of all selected channels upon Read of any digital-to-analog converter address, and (c) Simultaneous update of all selected channels upon receipt of an external signal.

EX1, SM1	Control analog output channels A0 and A1;
EX2, SM2	Control analog output channels A2 and A3;
EX3, SM3	Control analog output channels A4 and A5;
SM	Software-directed simultaneous-update mode: update happens on any analog output address read.
EX	Update on external pulse or on a low transition. If this update mode is selected, the external signal should be wired to the output connector pins 25, 24, and 23. These pins are allocated to Digital I/O port bits C4,5,6 and will be shared in this mode, which implies that 8255 PPI port C HI should be programmed either as an input or disabled. The external update can be disabled or enabled by three additional digital I/O lines allocated to port C bits 0,1, and 2. These lines might be controlled externally, or through the 8255 PPI if port C HI is selected as an output.
NONE	If switches are de-selected, update will happen automatically on second (high) byte Write to the digital-to-analog converter.

Installing the Card

Before installing the card, carefully read the Address Selection and Option Selection sections of this manual and configure the card according to your requirements. Be especially careful with Address Selection. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior.

To install the card:

1. Turn off computer power.
2. Remove the computer cover.
3. Remove the blank I/O backplate.
4. Set switches for desired options.
5. Select the base address on the card.
6. Install the card in an I/O expansion slot.
7. Install the I/O cable.
8. Inspect for proper fit of the card and cables, tighten screws.
9. Replace computer cover and apply power.

Software Installation

This package uses compression schemes to simplify installation and to permit use of a single diskette. A program is provided on your master disk to copy and expand the software package onto your floppy- or hard-drive. To begin the installation, place the software Master Diskette in a floppy drive and execute the INSTALL.EXE program.

For example, if you have placed the master disk in floppy drive **A**, you would type “a:install [ENTER]” to execute the installation program.

The installation program will ask you for various installation options, and will provide default settings. These default settings may be selected (by pressing ENTER) if they will work with your particular application and system setup, or you can respond to the questions with appropriate answers as needed.

When all of the installation options have been set, the program will expand the program files into the destination you have selected. Once this process is complete, please put your Master Diskette in a safe place as backup.

Chapter 3: Programming

The AOB6-P card uses 16 consecutive I/O addresses. The I/O address map is as follows:

ADDRESS	WRITE	READ
Base + 0	AO 0 Low byte **	Simultaneous update *
Base + 1	AO 0 High byte **	Simultaneous update *
Base + 2	AO 1 Low byte **	Simultaneous update *
Base + 3	AO 1 High byte **	Simultaneous update *
Base + 4	AO 2 Low byte **	Simultaneous update *
Base + 5	AO 2 High byte **	Simultaneous update *
Base + 6	AO 3 Low byte **	Simultaneous update *
Base + 7	AO 3 High byte **	Simultaneous update *
Base + 8	AO 4 Low byte **	Simultaneous update *
Base + 9	AO 4 High byte **	Simultaneous update *
Base + 10	AO 5 Low byte **	Simultaneous update *
Base + 11	AO 5 High byte **	Simultaneous update *
Base + 12	Dig. I/O Port A	Dig. I/O Port A
Base + 13	Dig. I/O Port B	Dig. I/O Port B
Base + 14	Dig. I/O Port C	Dig. I/O Port C
Base + 15	Dig. I/O Control ***	Illegal

Table 3-1: AOB6-P Card I/O Address Map

Notes:

* Analog output pairs selected by Analog Output Update switch will be simultaneously updated. See OPTION SELECTION - Analog Outputs Update.

** Data are written to the digital to analog converter in right-justified format; i.e.,

Byte	D7	D6	D5	D4	D3	D2	D1	D0
Low	B5	B6	B7	B8	B9	B10	B11	B12
High	X	X	X	X	B1	B2	B3	B4

For UNIPOLAR ranges:

0000 0000 0000 = ZERO
1000 0000 0000 = 1/2 SCALE
1111 1111 1111 = FULL SCALE

For BIPOLAR ranges:

0000 0000 0000 = - FULL SCALE
1000 0000 0000 = ZERO
1111 1111 1111 = +FULL SCALE

*** The Digital I/O Control Register is used to select the MODE of operation and to configure the 8255 PPI ports A, B, C HI and C LO.

D7	-	Mode set flag
D6, D5	-	Mode selection:
		00 = Mode 0, 01 = Mode 1, 1X = Mode 2
D4	-	Port A: 1 = input, 0 = output
D3	-	Port C upper: 1 = input, 0 = output
D2	-	Mode selection: 1 = Mode 1, 0 = Mode 0
D1	-	Port B: 1 = input, 0 = output
D0	-	Port C lower: 1 = input, 0 = output

For details of 8255 PPI operation, see Appendix C.

Chapter 4: Software

The AOB6-P card is straightforward to program. For example, the following procedure could be used:

To output an analog value with 12-bit resolution, a corresponding decimal number N between 0 and 4095 is calculated (2^12=4095).

N/4095= V(out)/V(full scale)

Then the number is split between high and low bytes as follows:

H%= INT (N/256)
L% = N - (H% * 256)

Next the data are written to the selected analog output channel. (See I/O Address Map.) In this example, we will assume analog output 0 (AO 0) :

OUT (BASE + 0), L%
OUT (BASE + 1), H%

For simplicity it was assumed that the Simultaneous Address Update switch is de-selected. Analog output 0 will change upon Write of high byte to (BASE + 1).

If the Simultaneous Address Update switch is used to select simultaneous software update (SM1, 2, 3 switches selected), then a Read from any address between BASE and BASE + 11 will cause the output to be updated.

A = INP (BASE + 0)

If External update is selected by the Simultaneous Address Update switch (EX1, 2, 3 switches selected), then update will wait for an external low-going transition on I/O connector pin 25 (AO 0 and AO 1), pin 24 (AO 2 and AO 3), and pin 23 (AO 4 and AO 5).

Mixing all update modes is allowed.

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Chapter 5: Calibration

Quick and easy calibration of the AOB6-P card can be done by using a menu-driven program on the Board Setup and Calibration diskette provided by I.C.S. Calibration is required whenever an analog output range is changed. In addition, periodic calibration of the card is recommended if it is used in extreme environmental conditions. The AOB6-P card uses very stable components but vibration or high/low temperature cycles might result in slight analog output errors.

Factory calibration and periodic calibration of the card includes adjustment of reference voltages +10V, +5V, and -2.5V. However, there is no need to perform that part of the calibration procedure if only changing ranges.

To calibrate the AOB6-P card, run the Board Setup and Calibration diskette and follow the screen prompts.

1. Select the card options and base address and install the card in the computer.
2. Measure the 10V reference voltage at the test point labelled +10V and adjust RP15, the 15-turn potentiometer marked +10V, until the voltage is 10.000 V. You will find a convenient GND test point immediately above U25. (There is no need to perform this step of the calibration procedure when changing ranges.)
3. Measure the +5V reference voltage at the test point labelled +5V and adjust RP14, the potentiometer marked +5V until the voltage is +5.0000 V. (There is no need to perform this step of the calibration procedure when changing ranges.)
4. Measure the -2.5V reference voltage at the test point labelled -2.5V and adjust RP13, the potentiometer marked -2.5V, until the voltage is -2.5000 V. (There is no need to perform this step of the calibration procedure when changing ranges.)
5. Select the DAC channel that you wish to calibrate or change range. Set the appropriate Output Range DIP Switch to the positions indicated by the computer display for the range that you desire. Measure the analog output voltage between the appropriate pin of the I/O Connector and Analog Ground I/O Connector Pin 13.

CHANNEL	I/O Pin
AO 0	18
AO 1	16
AO 2	14
AO 3	12
AO 4	2
AO 5	1

6. Select the "Set Offset" menu item in the computer display. Measure the DAC output voltage and adjust the 15-turn potentiometer marked OFFSET (for that DAC channel) until the output value is at minus full scale (or zero volts if a unipolar range was selected).
7. Select the "Set Gain" menu item in the computer display. Measure the DAC output voltage, and adjust the 15-turn potentiometer marked GAIN (for that DAC channel) until the output value is at plus full scale.
8. Repeat the steps 6 and 7 above to verify calibration.
9. Select the "Check Mid Scale" menu item in the computer, display. Measure the output voltage, and verify that the output value is correct. Calibration should be done on the range which will be used. No attempt at calibration should be made in noisy locations or with a noisy calibration setup.

Appendix A: Connector Pin Assignments

The analog and digital I/O signals are connected via a 37 pin D-type connector that extends through the back of the computer case. The mating connector is AMP type 747304-1 or equivalent. Pin assignments are as follows:

PIN	NAME	FUNCTION
1	AO 5	Analog Output channel 5
2	AO 4	Analog Output channel 4
3	PB7	Digital I/O Port B - 7
4	PB6	Digital I/O Port B - 6
5	PB5	Digital I/O Port B - 5
6	PB4	Digital I/O Port B - 4
7	PB3	Digital I/O Port B - 3
8	PB2	Digital I/O Port B - 2
9	PB1	Digital I/O Port B - 1
10	PB0	Digital I/O Port B - 0
11	DIG COM	Digital Common (Ground)
12	AO 3	Analog Output channel 3
13	RTN 3	Ground for Analog Channel 3
14	AO 2	Analog Output channel 2
15	RTN 2	Ground for Analog Channel 2
16	AO 1	Analog Output channel 1
17	RTN 1	Ground for Analog Channel 1
18	AO 0	Analog Output channel 0
19	RTN 0	Ground for Analog Channel 0
20	RTN 5	Ground for Analog Channel 5
21	RTN 4	Ground for Analog Channel 4
22	PC7	Digital I/O Port C-7
23	PC6	Digital I/O Port C-6 (Ext Update 3)
24	PC5	Digital I/O Port C-5 (Ext Update 2)
25	PC4	Digital I/O Port C-4 (Ext Update 1)
26	PC3	Digital I/O Port C-3
27	PC2	Digital I/O Port C-2 (Ext Update 3)
28	PC1	Digital I/O Port C-1 (Ext Update 2)
29	PC0	Digital I/O Port C-0 (Ext Update 1)
30	PA7	Digital I/O Port A-7
31	PA6	Digital I/O Port A-6
32	PA5	Digital I/O Port A-5
33	PA4	Digital I/O Port A-4
34	PA3	Digital I/O Port A-3
35	PA2	Digital I/O Port A-2
36	PA1	Digital I/O Port A-1
37	PA0	Digital I/O Port A-0

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Appendix B: Specifications

Analog Outputs:

Resolution

12 bits (0 to 4095 decimal)

Channels

Six

Voltage Output Ranges at 5mA max.

0.0 to 5.0 VDC
0.0 to 10.0 VDC
-2.5 to +2.5 VDC
-5.0 to +5.0 VDC
-10.0 to +10.0 VDC

Current Output Ranges with excitation voltage (8 - 36) VDC

1 to 5 mA
4 to 20 mA
0 to 50 mA*

* Addition of one 167 ohm resistor per channel is required. See OPTION SELECTION.

Digital to Analog Converter

AD-7537 monolithic chip, double buffered.
Relative Accuracy: ±1 LSB (includes nonlinearity).
Monotonicity: Guaranteed over operating temperature range.
Settling time: 50 usec to 0.01% for full scale step input.

Offset Temperature Drift

±1 ppm/C typ.
±3 ppm/C max.

Gain Temperature Drift

±1 ppm/C typ.
±5 ppm/C max.

Data Format: Right-justified, two bytes (8LSB's and 4MSB's).

Digital Inputs/Outputs

24 programmable digital input/ output lines.
(Ports A, B, C lo, and C hi).
8255 PPI Controller. All modes supported.

Inputs TTL, DTL, CMOS compatible

Logic Low: -0.5V to +0.8V.
Logic High: +2.0V to +5.0V.

Load Current: 10 uA.

Outputs TTL, DTL, CMOS compatible

Logic Low: 0.45V max. at 1.7mA sink current.
Logic High: 2.4V min. at -200uA source current. 1.5V min. at -1mA source current (Darlington drive not available from Port A).

Power Requirements

+5 VDC at 500mA max.
+12 VDC at 70mA max.
-12 VDC at 60mA max.

Environmental

Operating Temperature: 0 to +60°C.
Storage Temperature: -20 to +85°C.
Humidity: 5% to 95% non condensing.

Size

13.375 inches. Install in a full-size slot.

Appendix C: Programmable Peripheral Interface Data Sheets

The data sheet in this Appendix is provided to help your understanding of the 8255-5 PPI which is made by a number of companies. These sheets are reprinted with permission of Mitsubishi Electric Corp. (Copyright 1987).

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Appendix D: Sample Program

The AOB6-P software package includes several sample program in BASIC, C, and Turbo Pascal. These programs can be used to generate sine, triangular, and sawtooth waveforms. If you wish to write your own routines to generate some other waveform, block copy one of the waveform "procedures" and change the assignment statements that set the variable "temp" by introducing your own algorithm.

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AOB6-P

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EN 50081-1:1992 Emissions, Generic Requirements.

-EN 55022 Measurement of radio interference characteristics of information technology equipment.

EN 50082-1:1992 Immunity, Generic Requirements.

-IEC 801-2:1984 Immunity for AC lines, transients, common, and differential mode.
-IEC 801-3:1984 Immunity for radiated electromagnetic fields.
-IEC 801-4:1988 Immunity for AC and I/O lines, fast transient common mode.

EN 60950:1992 Safety of Information Technology Equipment.

Information supporting this declaration is contained in the applicable Technical Construction file available from:

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Z.A. de Courtaboeuf
16, Avenue du Québec
B.P. 712
91961 LES ULIS Cedex

August 28, 1997
San Diego, CA

Mr. Steven R. Peltier
President & Chief Executive Officer

BUG REPORT

While we have tried to assure this manual is error free, it is a fact of life that works of man have errors. We request you to detail any errors you find on this BUG REPORT and return it to us. We will correct the errors/problems and send you a new manual as soon as available. Please return to:

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