INDUSTRIAL COMPUTER SOURCE®

# Model PCDIO Series
# Product Manual

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# Table of Contents

## List of Figures



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# Chapter 1: Description

## General

The PCDIO family consists of generalized multiple channel digital I/O boards providing buffered, user selectable inputs and outputs based on the 8255 PIO by Intel. The I/O is software selectable in groups of 8 (groups of 4 for Port C of each 8255) for either input or output.

The boards are pin compatible with popular industrial solid state I/O racks and modules such as the PB8, PB16A, PB24 and those manufactured by Opto 22, Grayhill, Gordos, and others. The PCDIO's provide a 50-pin male IDC connector for each 8255, which will interface to 8, 16 and 24 position OPTO racks. Because the I/O are programmable, both input and output modules can be mixed on one rack in 8 (or 4) channel groups. Five volts to power a single 8-channel rack is available on the board and is fused. If a large relay rack is required, an external +5VDC power source is required. Most computers have sufficient power available for multiple racks, however, the power must be taken directly from the power supply, not through the PCDIO the board.

The boards use LS245 buffers which will provide 15mA of source current and 24mA of sink current (48mA with specially requested buffers.)

On the PCDIO24-P and PCDIO216-P cards, two of the I/O lines of each 8255 may be used to generate a hardware interrupt. The inputs are buffered and can be connected to IRQ 2, thru 7 on the PCDIO24-P, and the same plus 10 thru 12, 14, and 15 on the PCDIO216-P. Only one hardware interrupt connection per board is allowed although multiple 8255s may share an interrupt line.

**Features**

- 24 to 216 Channels of Digital Input/Output
- Four and Eight Bit Groups Independently Selectable for I/O
- All I/O Lines Buffered on Board
- Hysteresis on I/O Lines
- All lines pulled up to +5Volts
- OPTO-22 Compatible 50 Pin Connector
- Positive True Logic
- Interrupt and Interrupt Disable Capability (PCDIO24-P, and PCDIO216-P)
- Fused on Board +5V Supply Available for User (PCDIO24-P only)

**Applications**

- Security Systems, Energy Management
- Relay Monitoring and Control
- Parallel Data Transfer to PC
- Sensing Switches or Signals, or TTL, DTL, CMOS Logic
- Driving Indicator Lights or Recorders

# Specifications

**Size**

| | |
|---|---|
| PCDIO24-P | 5.5"(13.97cm)L |
| PCDIO48-P | 6.75"(17.14cm)L |
| PCDIO72-P | 9"(22.86cm)L |
| PCDIO120-P | 13.25"(33.65cm)L |
| PCDIO216-P | 13.25"(33.65cm)L |

**Environmental**

| | |
|---|---|
| Operating Temperature | 0-60° C |
| Storage Temperature | -50° to +120° C |

**Humidity**

0 to 90% non-condensing

**Agency Approvals**

CE Conformity with:

EU EMC Directive 89/336/EEC

EU Low Voltage Directive 72/23/EEC

CE

## Inputs and Outputs

- 24, 48, 72, 120, or 216 Input/Output lines
- Interrupt and interrupt enable lines (PCDIO24-P and PCDIO216-P)
- Hysteresis at inputs to improve noise immunity
- All Outputs and Inputs are TTL/DTL compatible with pull-ups installed. They are CMOS and contact closure compatible. Pull-ups provide 1mA of current (4.7K pull-up resistors)

**Output Source Current (output high)**

15mA

**Output Sink Current (output low)**

24mA (48 mA by replacing 74LS245 buffers with 74S245 buffers (ports A and B) and 74LS243 buffers with 74s243 buffers (port c)

**Address**

4 to 36 Bytes, mapped within 200-3FF range of I/O address space

**Power Output**

+5V Power available to user, (1A fuse on PCIDO24-P board)

**I/O Connector**

A single 50 Pin header for each 8255 (24 channels)

# PCDIO Block Diagram

The block diagram of the PCDIO24-P shows the typical 24 channel circuitry for a single 8255. The PCDIO48-P, PCDIO72-P, PCDIO120-P, and PCDIO216-P are similar and repeat this circuitry for each additional 8255: (interrupt line only on PCDIO24-P, and PCDIO216-P).

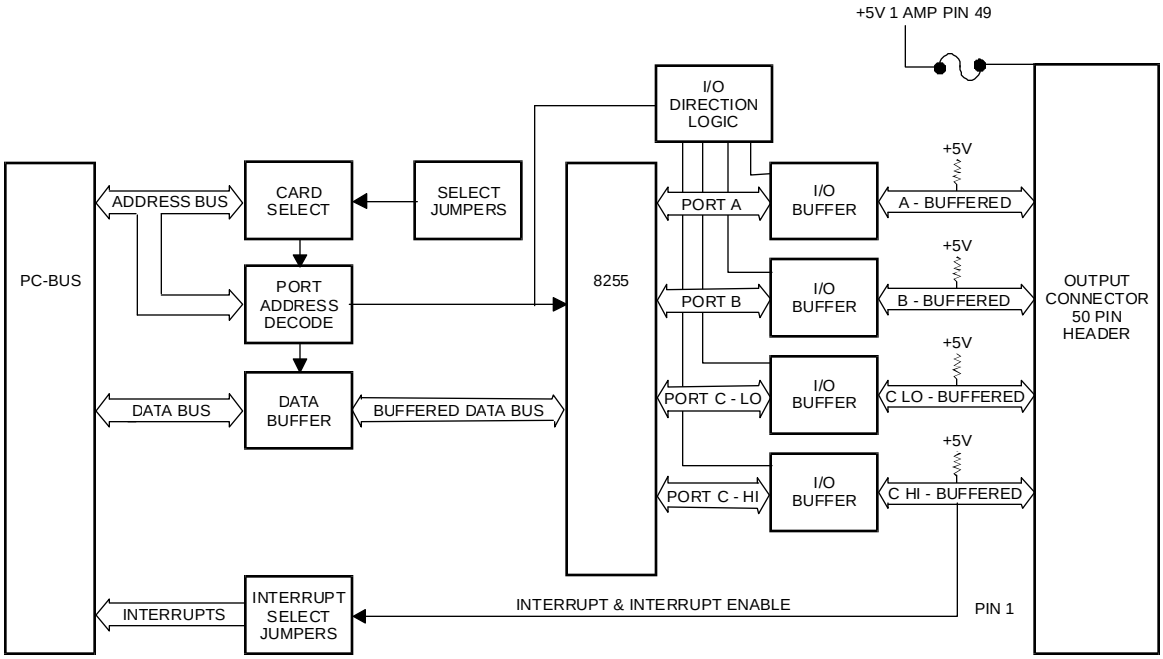


**Figure 1: PCDIO24-P Block Diagram**

## Board Layout Diagrams

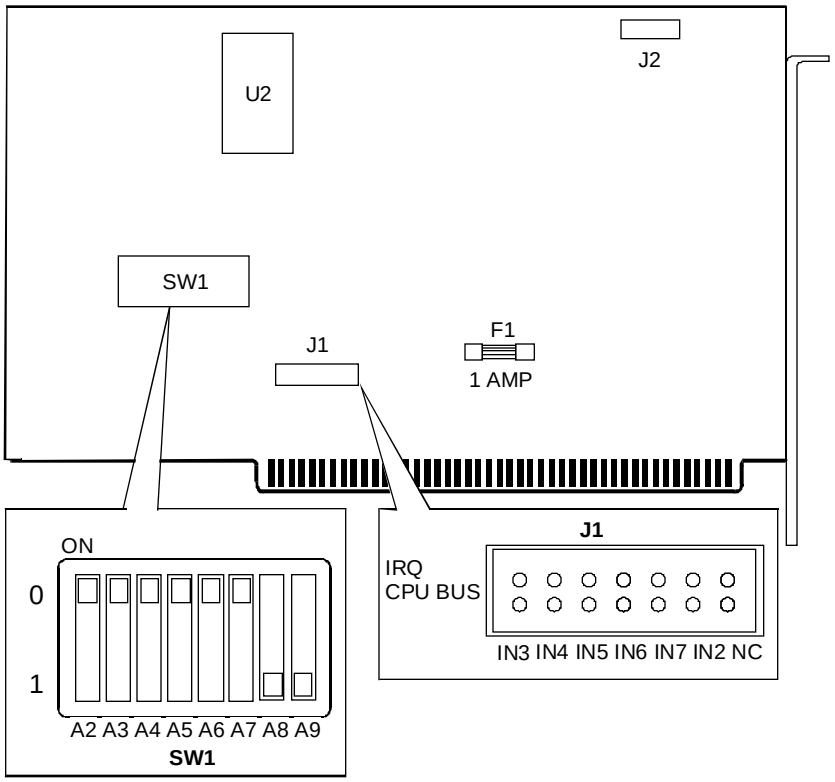


**Figure 2: PCDIO24-P Board Layout**

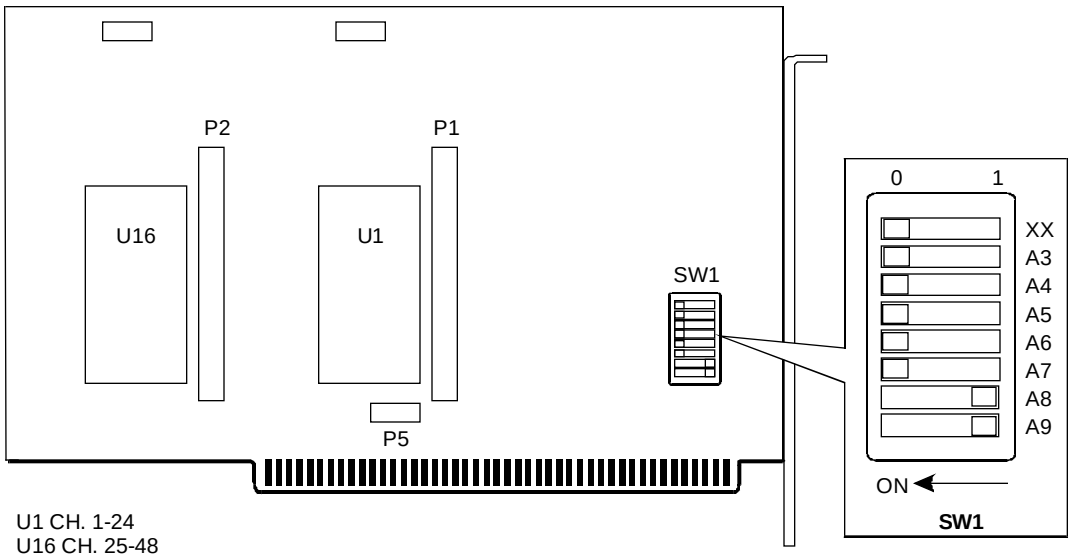


**Figure 3: PCDIO48-P Board Layout**

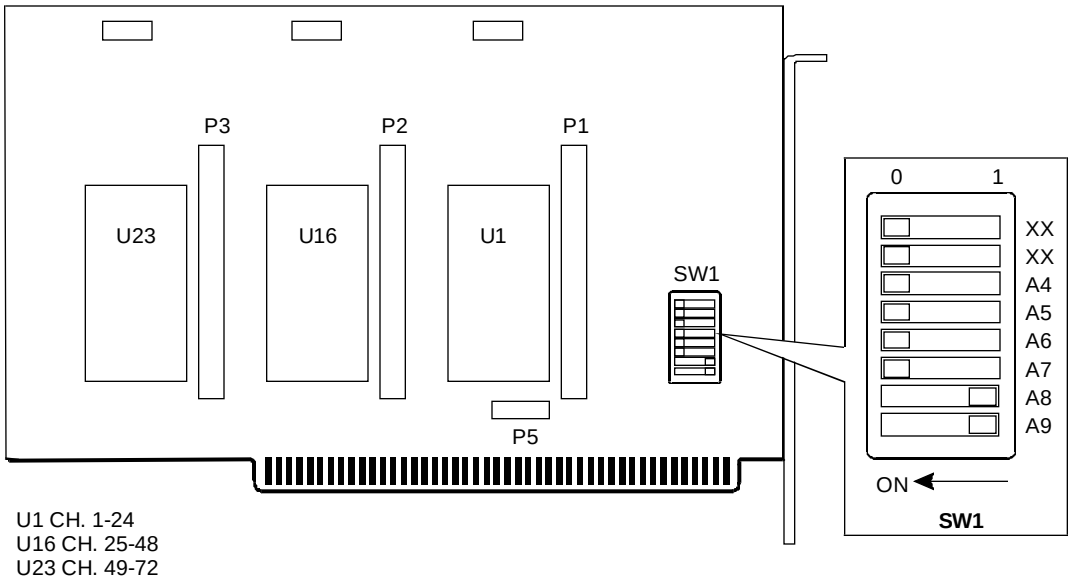


**Figure 4: PCDIO72-P Board Layout**

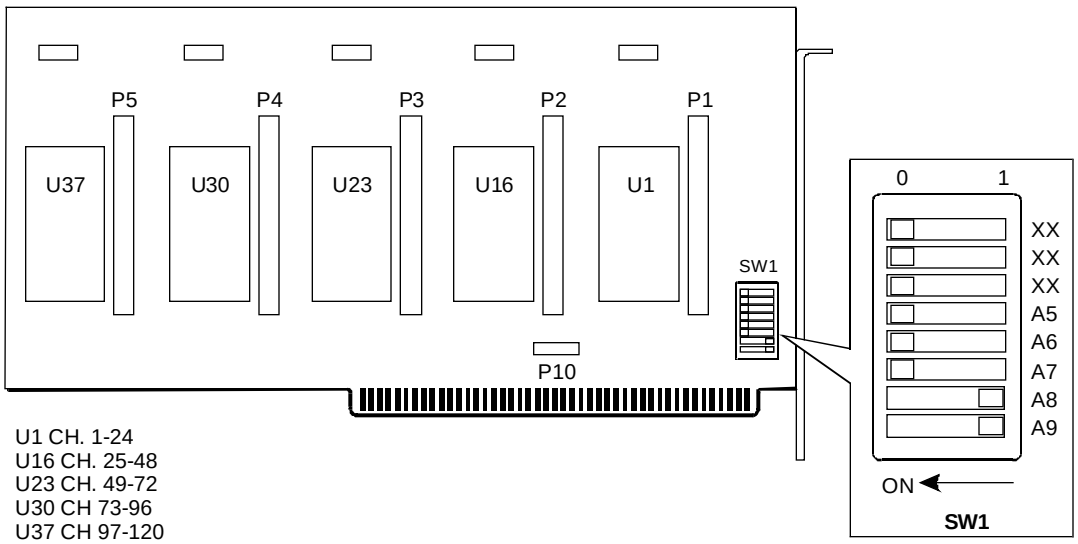


**Figure 5: PCDIO120-P Board Layout**

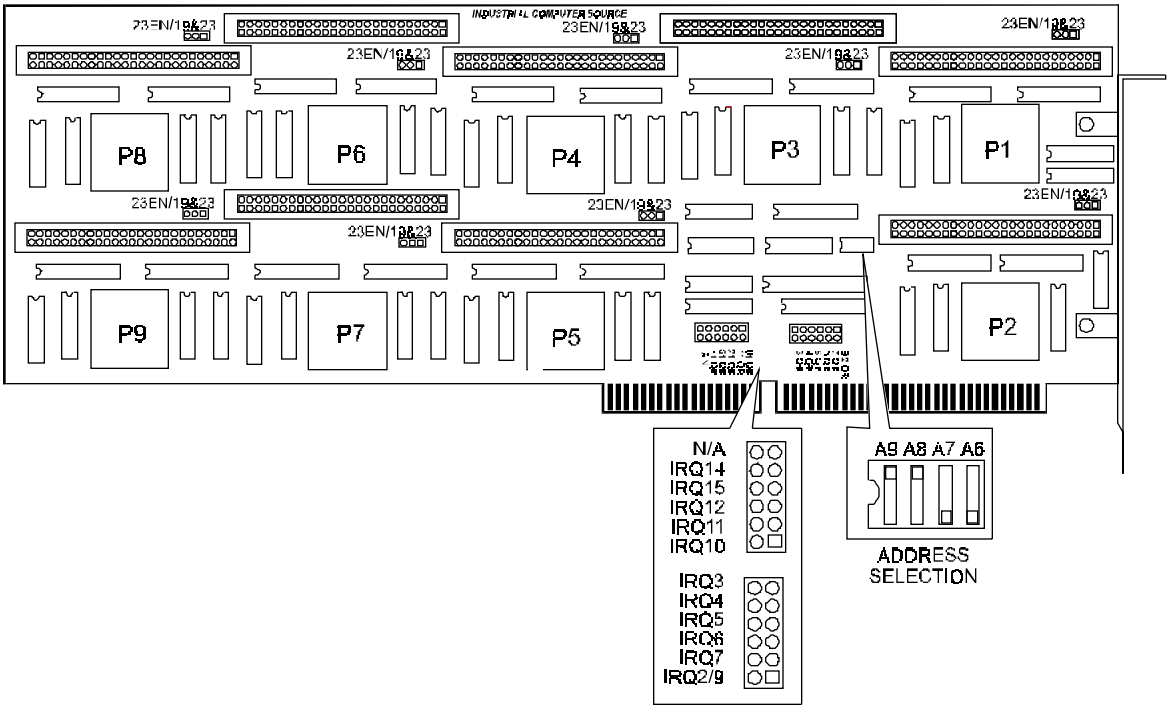


**Figure 6: PCDIO216-P Board Layout**

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# Chapter 2: Installation

The PCDIOs function as part of a complete computer monitoring or controlling system.

**CAUTION!**

Installing or removing any accessory board with power applied may cause physical damage to the plug-in board, the computer or both. Turn off the power before installing or removing I/O boards.

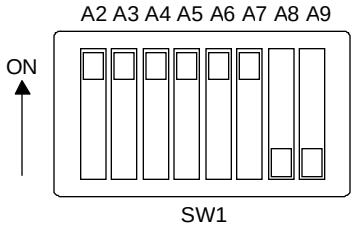
## Selecting the Base Address

The PCDIOs require consecutive address locations in the I/O space per the following table.

| Model | I/O Bytes | Boundaries |
|---|---|---|
| PCDIO24-P | 4 | 4 Byte |
| PCDIO48-P | 8 | 8 Byte |
| PCDIO72-P | 12 | 16 Byte |
| PCDIO120-P | 20 | 32 Byte |
| PCDIO216-P | 36 | 64 Byte |

Carefully review the address selection reference table before selecting the card address and then perform the Installation Precheck Procedure (described later in this Chapter), to determine if that address is in fact free. If the addresses of two installed items overlap, you will experience unpredictable computer behavior.

Some I/O address locations will be occupied by internal I/O and your other peripheral cards. To provide flexibility in avoiding conflict with these devices, the I/O board address can be set by the Base Address D.I.P. switch to be on a 4 to 64 byte boundary anywhere in the IBM PC decoded I/O space. This I/O address space extends from decimal 512-1023 (Hex 200-3FF). Such a large space allows use of more than one PCDIO in a single computer.



## Input/Output Selection

The 8255 PIO used as the heart of the PCDIO provides 24 bits of digital Input or Output. The chip is divided into three 8-bit ports A, B, and C. Ports A and B are each 8 bits while port C can be 8 bit or can be divided into two 4-bit ports, C- Upper and C-Lower.

The buffer direction, input or output, is set when the 8255 Control Register at Base Address + 3 is configured. The PCDIO power-on default defines all ports as input ports.

**Note:** Because the buffers are not simultaneously bi-directional, only Mode 0 is supported with the 74LS245 buffers installed. See Chapter 3 for a description of the three operating modes of the 8255 chip.

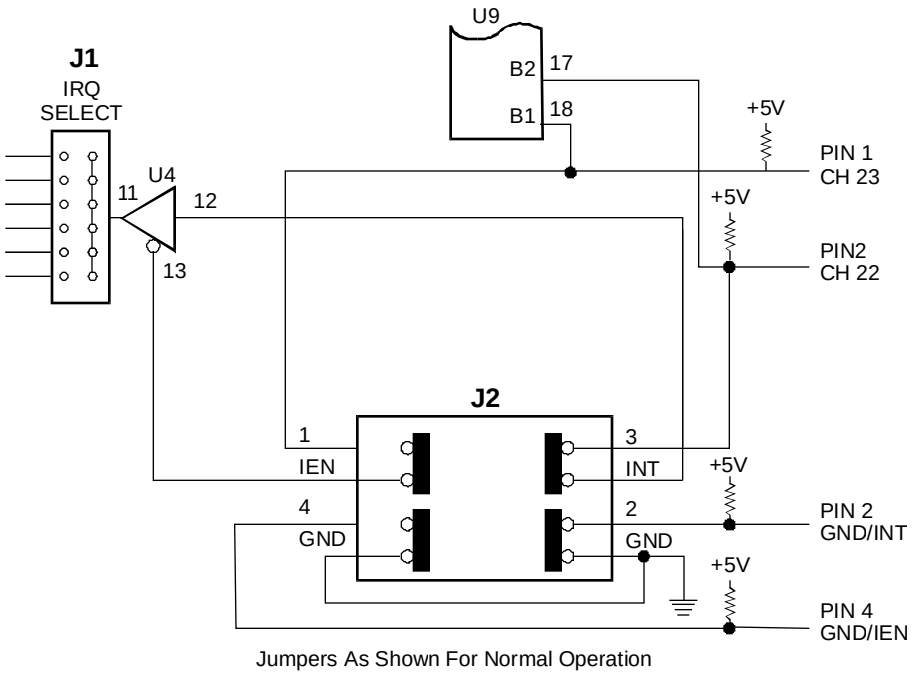
**CAUTION!**

The user should be careful to set the control port and buffer direction to agree with externally connected devices. Setting a port connected to an input device as an output port may damage the PCDIO, the external device or both.

## Interrupts

The PCDIO24-P provides for input channels 22 and 23 to generate hardware interrupts. These interrupts can be directed to any of the Interrupt Request Lines (IRQ2, 3, 4, 5, 6, and 7) available on the 8-bit PC/XT/AT I/O expansion bus.

Pin-1 (Channel 23) is configured as an INTERRUPT ENABLE and Pin-3 (Channel 22) is the INTERRUPT INPUT on the 50 pin header connector. The INTERRUPT ENABLE pin is pulled-up, disabling the interrupt as the default.




Jumpers As Shown For Normal Operation

For Interrupt Operation:
4 to IEN = External Interrupt Enable
2 to INT = External Interrupt Input

To use the interrupts, simply insert the appropriate IRQ jumper to select the desired interrupt channel. To determine which input generated the interrupt, read PORT C UPPER, bits 6 and 7, to read the current state of the inputs. Note that the inputs are not latched and no "first event" trapping is provided to determine which input was active.

Jumper block J2 (not populated) allows the user to "customize" the interrupt inputs to use pins 2 and 4 of the I/O connector. These jumpers are not normally used and interested users are directed to the schematic for additional details. Traces on the PCB must be cut to use these jumpers. See Figure 4 for details of the circuit.

**Note:** If you do decide to cut the jumpers for your application, be advised that the board is no longer returnable under the Industrial Computer Source 30 Day Return Policy. The warranty will still be valid presuming adequate care is taken in performing the modification and the other areas of the board are not damaged.

You should also be aware that an interrupt will be generated if the IRQ jumper is inserted and PORT C UPPER is used as an output. This feature could be used to test an interrupt routine without external connections being required. If you need further information or instruction on the use of interrupts, please refer to the "IBM Technical Reference Manual" for details on usage and programming. That subject is beyond the scope of this manual.

## Connector Pin Assignments

A 50 pin ribbon cable header (represented by the shaded area below), Model Winchester 86-50-13-2 is used for interfacing to I/O. For mating connector use Winchester 50 pin connector with strain relief part no. 81-50-112 or equivalent. Connector pin assignments are listed below.

| ASSIGNMENT | CHANNEL | I/O | PIN | PIN | ASSIGNMENT |
|---|---|---|---|---|---|
| Port C HIGH | PC7 [1] | 23 | 1 | 2 | GROUND [2] |
| Port C HIGH | PC6 [3] | 22 | 3 | 4 | GROUND [4] |
| Port C HIGH | PC5 | 21 | 5 | 6 | GROUND |
| Port C HIGH | PC4 | 20 | 7 | 8 | GROUND |
| Port C LOW | PC3[5] | 19 | 9 | 10 | GROUND |
| Port C LOW | PC2 | 18 | 11 | 12 | GROUND |
| Port C LOW | PC1 | 17 | 13 | 14 | GROUND |
| Port C LOW | PC0 | 16 | 15 | 16 | GROUND |
| Port B | PB7 | 15 | 17 | 18 | GROUND |
| Port B | PB6 | 14 | 19 | 20 | GROUND |
| Port B | PB5 | 13 | 21 | 22 | GROUND |
| Port B | PB4 | 12 | 23 | 24 | GROUND |
| Port B | PB3 | 11 | 25 | 26 | GROUND |
| Port B | PB2 | 10 | 27 | 28 | GROUND |
| Port B | PB1 | 9 | 29 | 30 | GROUND |
| Port B | PB0 | 8 | 31 | 32 | GROUND |
| Port A | PA7 | 7 | 33 | 34 | GROUND |
| Port A | PA6 | 6 | 35 | 36 | GROUND |
| Port A | PA5 | 5 | 37 | 48 | GROUND |
| Port A | PA4 | 4 | 39 | 40 | GROUND |
| Port A | PA3 | 3 | 41 | 42 | GROUND |
| Port A | PA2 | 2 | 43 | 44 | GROUND |
| Port A | PA1 | 1 | 45 | 46 | GROUND |
| Port A | PA0 | 0 | 47 | 48 | GROUND |
| + 5VDC | (1A Fuse) | | 49 | 50 | GROUND |

**Notes:**

1. This line is factory configured as an Interrupt Enable for all cards.
2. This line could be configured as an Interrupt Enable for PCDIO24-P (see Figure 3).
3. This line is factory configured as an User Interrupt for the PCDIO24-P.
4. This line could be configured as an User Interrupt (See Figure 3).
5. This line is factory configured as a user interrupt for the PCDIO48-P, PCDIO72-P, and PCDIO120-P.

## Setting the Base Address

| Hex Range | Usage |
|---|---|
| 000-0FF | Internal System - Not Usable |
| 1F0-1FF | AT Hard Disk |
| 200-207 | Game Control |
| 278-27F | Parallel Port (LPT2) |
| 238-23B | Bus Mouse |
| 2E8-2EF | Asynchronous Communications (COM4) |
| 2F8-2FF | Asynchronous Communications (COM2) |
| 300-31F | Prototype Card |
| 320-32F | XT Hard Disk |
| 378-37F | Parallel Port (LPT1) |
| 380-38F | SDLC Communications |
| 3A0-3AF | SDLC Communications |
| 3B0-3BB | MDA |
| 3BC-3BF | Alt. Parrallel Port |
| 3C0-3CF | EGA |
| 3DO-3DF | CGA |
| 3E8-3EF | Asynchronous Communications (COM3) |
| 3F0-3F7 | Floppy Disk |
| 3F8-3FF | Asynchronous Communications (COM1) |

| | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 |
|---|---|---|---|---|---|---|---|---|
| **200H** | OFF | ON | ON | ON | ON | ON | ON | ON |
| **210H** | OFF | ON | ON | ON | ON | OFF | ON | ON |
| **220H** | OFF | ON | ON | ON | OFF | ON | ON | ON |
| **300H** | OFF | OFF | ON | ON | ON | ON | ON | ON |
| **310H** | OFF | OFF | ON | ON | ON | OFF | ON | ON |
| **320H** | OFF | OFF | ON | ON | OFF | ON | ON | ON |
| **350H** | OFF | OFF | ON | OFF | ON | OFF | ON | ON |

| **Address Line** | **A11** | **A10** | **A9** | **A8** | **A7** | **A6** | **A5** | **A4** | **A3** | **A2** | **A1** | **A0** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Binary** | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Hex** | 3 | | | | 0 | | | | 0 | | | |
| **Switch Setting** | | | OFF | OFF | ON | ON | ON | ON | ON | ON | | |

**Note:** The above tables are for reference only; not all boards have all theses switches available, however, the addressing scheme is similar for all the PCDIO boards. Carefully review the address selection reference table before selecting the card address and then perform the Installation Precheck Procedure to determine if that address is in fact free. If the addresses of two installed items overlap, you will experience unpredictable computer behavior.

## Installation Precheck Procedure

The precheck procedure is designed to help you determine if the address you have selected for the board is actually free for use. In the following example we are testing for an address of hex 300, but any other address may be substituted.

1. Type DEBUG at the DOS prompt and the press the Enter key. The DOS directory must be in your path statement or you must change to the DOS subdirectory before running this application. The DEBUG "-" prompt is displayed.

2. Type **i 300** at the DEBUG "-" prompt and press the Enter key. This reads I/O address H300. DEBUG returns an **FF** if the address is not currently in use. If a value other than **FF** is returned, the address is being used by another board. Try each desired address until an **FF** is returned. For information about the various functions available through DEBUG, simply type a **?** at the prompt and press the Enter key.

3. Repeat step 2 for all the consecutive address space required by your PCDIO board. For example, if **300** checked out, check **301**, **302**, etc. Each of these addresses should also return an **FF**.

4. After you have finished checking each address, type **q** and press the Enter key to exit DEBUG.

5. Turn off the computer in preparation for installing the circuit board. If you haven't already done so, set the address switches in accordance with the directions in the previous section.

## Installing the Board

**CAUTION!**

Be sure to turn off the power to the computer before installing the board. Failure to do so could cause damage to the board or computer, invalidating the warranty

To install the board, perform the following steps:

1. Turn off the computer and remove the cover of the case.
2. Select an empty, standard size slot and remove the screw at the top of the slot's backplate.
3. Remove the backplate.
4. Plug all necessary cables into the PCDIO board
5. Plug the board into the empty slot. Ensure that the board is firmly seated in the slot.
6. Reinstall the screw removed in step 2. Ensure that the board is securely fastened in place.
7. Reinstall the cover of the case.

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# Chapter 3: Programming

The PCDIOs use the 8255 PIO to provide the 24 bits of Input and Output. These 24 bits are divided into three 8-bit ports: A, B and C. Port C is further divided into two 4-bit ports:

C-Lower and C-Upper.

The outputs of the PCDIOs are positive true, i.e. a 1 written to a bit will cause it go high. This high output will turn OFF a solid state relay attached to that channel. To turn a relay ON, write a 0 to the appropriate bit.

The 8255 provides a CONTROL REGISTER at the card's BASE ADDRESS+3. This is a WRITE ONLY, 8-bit register and is used to set the MODE and DIRECTION of these 4 ports (A, B, C-Upper, C-Lower). On Power-Up or Reset, all 24 I/O lines are set as inputs. The 8255 should be configured by writing to the CONTROL REGISTER before the chip's ports are accessed, even as inputs.

**NOTE:**

Setting a port as an output port by writing to the control register initializes the outputs as all 0's or LOW. If attached to a relay rack such as the PB24, relays attached to these ports will be turned ON until 1's are written to the appropriate output bits to turn them off.

## Register Access

Each 8255 section is mapped into 4 bytes in the IBM I/O space. The address definitions are:

| | | | |
|---|---|---|---|
| Base Address + | 0 | Port A | Read/Write |
| | 1 | Port B | Read/Write |
| | 2 | Port C | Read/Write |
| | 3 | Control Register | Write Only |

For the additional ports on the PCDIO48-P, PCDIO72-P, PCDIO120-P, and PCDIO216-P add 4 to the Base Address for each additional 8255. For example, the third port set on the PCDIO120-P would be channels 49 through 72, the 24 bits of the third 8255. The ports of that chip will be Base Address + 8 through Base Address + 11 for Port A through the Control Register respectively.

To access the board from BASIC, for example:

1. Determine which ports are to be for input and which for output. Determine the proper bit pattern to write to the CONTROL REGISTER as discussed in the following section.

For example, for a configuration of:

| | |
|---|---|
| Port A | Input |
| Port B | Output |
| Port C-Upper | Input |
| Port C-Lower | Output |

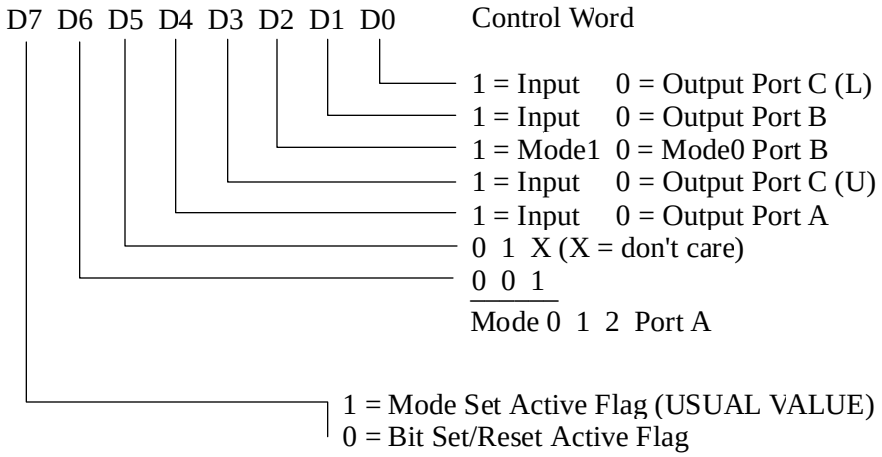
The bit pattern would be 1001 1000 (Hex 98). Use the BASIC OUT statement to write to the CONTROL REGISTER (refer to the next section for more detail on the CONTROL REGISTER):

```
10 BASEADDR = &H300
20 OUT BASEADDR+3, &H98
30 X=INP(BASEADDR):Y=INP(BASEADDR+2)        'READ PORTS A,C
40 PRINT X;Y                                'PRINT THE VALUES
50 OUT BASEADDR+1,255                       'TURN OFF PORT B 'RELAYS
60 OUT BASEADDR+2,15                        'TURN ON 4 BITS OF C
```

## Control Register

Before the 8255 can be used, it must be configured. Each of the 8-bit ports A, B, and C can be selected as input or output ports (port C can also be selected as a control port if the buffers have been replaced with wire jumpers). Remember, the 8255 power-up default mode is with all ports configured for inputs and the CONTROL REGISTER should be configured even if this is the mode you require.

### 8255 Mode Definition Format



## Modes of Operation

The 8255 offers 3 MODES of operation as set by bits 3, 6 and 7. Bit 3 sets the mode for port B and bits 6 & 7 for port A. Port C has no independent modes. The 8255 has several input/output modes and the user is directed to the 8255 data sheet (refer to Appendix A) for complete programming details. The following information will provide sufficient information for the majority of users.

Modes 1 and 2 require bi-directional I/O which cannot be supported with the buffered I/O of the PCDIOs. This information is given only as a point of reference to help the user understand the 8255 datasheet. If Modes 1 or 2 are required for an application, Industrial Computer Source offers an un-buffered, 24 channel card called the DIO24-P. All three modes are supported on the DIO24-P as all I/O connects directly to the 8255. These modes can also be implemented on the PCDIO's by removing the 74LS243 I/O buffers from the board. Replace the buffers with wired headers to carry the 8255 signals through the sockets to the edge connector. See the schematics located at the end of this manual for wiring details. The modes are described below (Mode 1 and 2 descriptions are provided for information only):

MODE 0 - Basic Input/Output - This is the standard PCDIO mode

MODE 1 - Strobed Input/Output

MODE 2 - Bi-directional Bus

**Note:** If you choose to remove the buffers from the board, your warranty will not be voided as long as proper care is taken in removing the ICs. If the board is physically damaged in the process, the warranty will be voided.

**MODE 0**

This functional configuration provides simple input and output operations for each of the three ports. No “handshaking” is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output combinations are possible in this mode

**MODE 1**

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or “handshaking” signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these “handshaking” signals.

Mode 1 Basic Functional Definitions

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port
- The 8-bit data port can be either input or output. Both inputs and outputs are latched
- The 4-bit port is used for control and status of the 8-bit data port

**MODE 2**

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). “Handshaking” signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions

- Used in Group A only
- One 8-bit, bidirectional bus port (Port A) and a 5-bit control port (Port C)
- Both inputs and outputs are latched
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A)

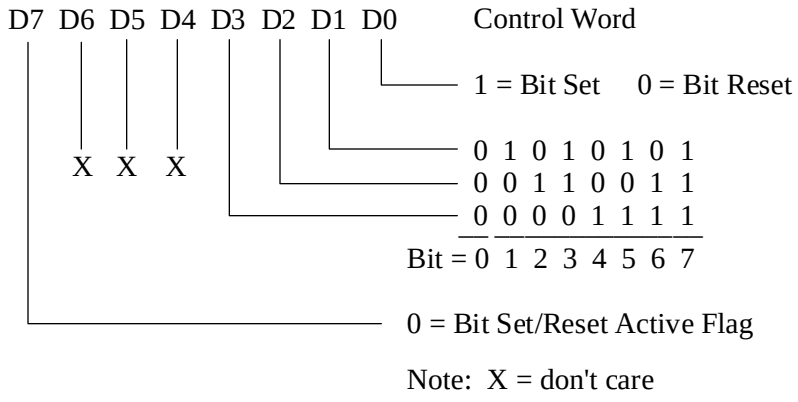
## Bit Set/Reset

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in control-based applications. When Port C is being used as status/ control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

**Note:** This mode required disabling the buffers by replacing the buffers with wire jumpers.

Bit 7 controls the Bit Set/Reset function. When bit 7=1 the port is a control port. When set to 0 the Bit Set/Reset function is used.

### Bit Set/Reset Format




## Peek and Poke Driver for Windows 95/NT

This driver allows developers to write Win32 programs which access hardware I/O ports and physical memory. This should allow easier testing of hardware components since they can be accessed without the use of a specific driver.

It should be noted that this driver will give application level access to areas of the hardware and memory which can quite easily crash the operating system or even corrupt data. Care needs to be taken to only access known memory or I/O ports.

### Using The Library

There are two libraries that can be used to ease use of the Peek and Poke driver. They are pplib95.lib and pplibnt.lib. They are used for Windows 95 and Windows NT respectively. These libraries provide I/O routines familiar to those who have used Microsoft compilers in the past.

To use a library, add pplib95.lib or pplibnt.lib to your link, whichever is appropriate for the target OS. Include pplib95.h or pplibnt.h in the C/C++ file you will be accessing the functions from. These libraries are compatible with all Microsoft compilers. NOTE: These libraries are not thread safe.

The following is a list of the functions provided by the library.

| Function | Description |
|---|---|
| BOOL ics_pp_open ( void ) | Opens the Peek and Poke driver. Returns TRUE if successful. This must be called before any calls are made to the other library functions. |
| void ics_pp_close ( void ) | Closes the driver. Should be called before the application exits. |
| void *ics_pp_make_pointer (int page, int length) | This function is used to allow access to a particular region of physical memory by a Win32 application. page is the starting page of the physical memory. length is the size of the region in pages. For example, for a pointer to a region of physical memory starting at 0xA0000 and 64k long: void *ptr = ics_pp_make_pointer (0xA0, 0x10); The pointer can then be treated as a standard C/C++ pointer. NOTE: Be sure to release this memory region back to the system with a call to ics_pp_release_pointer. (See Below.) |
| void ics_pp_release_pointer (void *address, int length) | This function is used to release a memory mapping made with ics_pp_make_pointer. It is important to release such pointers back to the system. Failure to do so could affect the way the system runs even after the application has exited. address is the address that was returned by the ics_pp_make_pointer function. length is the size of the mapped region in pages. |
| int _outp (USHORT port, int data) USHORT _outpw (USHORT port, USHORT data) ULONG _outpl (USHORT port, ULONG data) | These functions output data to the given port. Use _outp for byte width, _outpw for word width, and _outpl for double word width. |
| Int _inp (USHORT port) USHORT _inpw (USHORT port) ULONG _inpl (USHORT port) | These functions return data input from the given port. Use _inp for byte width, _inpw for word width, and _inpl for double word width. |

## PeekPoke Driver for Windows NT Installation

This driver allows developers to write WinNT programs which access hardware I/O ports and physical memory.

### Installing the Windows NT PeekPoke Driver

Under Windows NT 3.51:

- From the Program Manager, click on File->Run.
- Type a:\setup and press OK.

From Windows NT 4.0

- From the Start Menu, select Run.
- Type a:\setup and press OK.

The InstallShield installer will initialize and run. Follow the on-screen instructions. You will need to provide one piece of information:

- The destination path for the driver files.

When the files are transferred, you will be asked if you want to reboot the computer. The drivers will not work until after a reboot.

## PeekPoke Driver for Windows 95 Installation

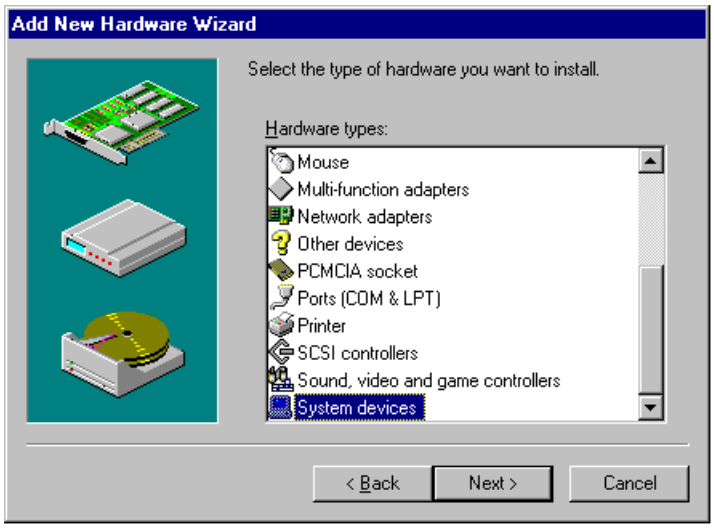
This driver allows developers to write Win95 programs which access hardware I/O ports and physical memory.

### Installing the Windows 95 PeekPoke Driver

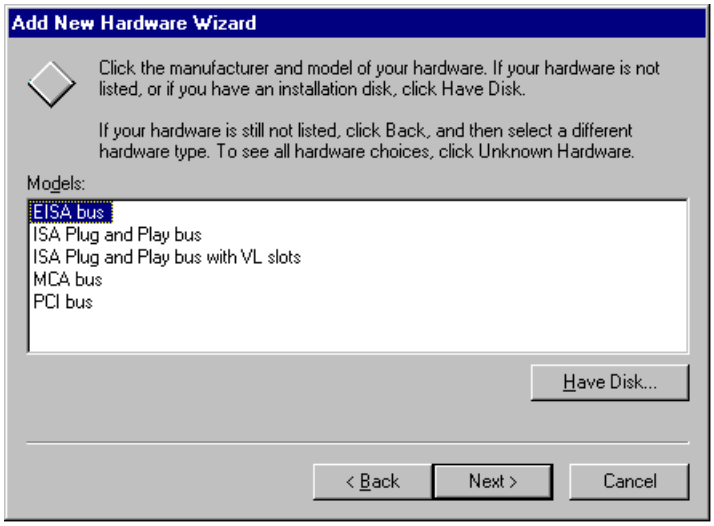
- From the Start Menu, select Settings->Control Panel.
- From the Control Panel, select Add New Hardware.


- Click the Next button.

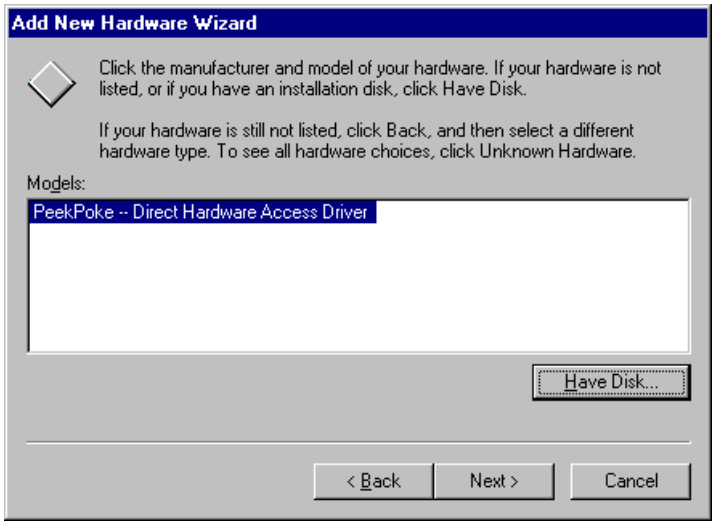

- Answer “No” to the question, “Do you want Windows to search for you new hardware?”
- Press the Next button.




- Scroll the hardware types list down and select the “System devices” type.
- Press the Next button.




- Press the Have Disk button.
- Insert your disk labeled “Windows 95 PeekPoke Driver Disk.”
- Make sure “A:\” is selected as the source.
- Press OK.




- The model “PeekPoke – Direct Hardware Access Driver” should be selected in the Models box.
- Press the Next button.
- Windows 95 will copy the driver’s files onto your system.
- Press the Finish button.
- At this point, you will need to shutdown and reboot your machine for the changes to take effect.

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# Chapter 4: Application

## Connecting Optically Isolated Relay Racks

The PCDIOs are pin compatible with 8, 16 and 24 position Industrial Solid State Relay Racks. In addition, the 5 volts required to operate a rack is available on the PCDIOs and is fused at 1 amp on the PCDIO24-P.

To connect the relay rack such as the PB8, PB16A, PB24, or racks manufactured by OPTO22, GORDOS and others, connect a cable, such as the Industrial Computer Source CAB50-6 or CAB50-10 from the card to the rack. The relay racks can be powered from an external voltage source or up to eight (8) relays can be powered from the PCDIO.

**Note:** If powered by the card, a jumper must be inserted on the relay rack to connect Pin 49 (+5 volts) to the rack.

## Using Multiple Relay Racks

The +5VDC power available from the PCDIO is supplied by your computer's power supply. If you need to supply power to more than eight (8) relays, you will have to use an external +5VDC supply or use a +5VDC connector from the computer power supply.

The PCDIO can be programmed for inputs and outputs. The only limitation to the I/O mix installed on a relay rack is that they must be in groups of 8 (input and output 0 and the PCDIO ports must be programmed to match the module type to which they are connected.

**CAUTION!**

The user should be careful that OPTO **INPUT** modules are not connected to ports on the PCDIO programmed as **OUTPUTS**. Such a condition would lead to the modules and card "fighting" each other leading to high currents in the devices and possible damage to the module, card or both.

It will not hurt to have OUTPUT modules connected to ports configured as INPUTS. The two devices will be "pulling" against each other, not leading to the high currents mentioned in the above caution.

It should also be noted that with the standard cable pin outs, the PB8 is connected to port A, the PB16 is connected to ports A & B, and PB24 to ports A, B, & C. This means that PB8 can't be split between input and output; it must be 8 of one type. A PB16, on the other hand, must be 8 of one type and 8 of another type or all 16 the same (it can't be 4 of one and 12 of the other).

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# Chapter 5: Maintenance

## How to remain CE Compliant

In order for machines to remain CE compliant, only CE compliant parts may be used. To keep a chassis compliant it must contain only compliant cards, and for cards to remain compliant they must be used in compliant chassis. Any modifications made to the equipment may affect the CE compliance standards and should not be done unless approved in writing by Industrial Computer Source.

The PCDIO Family is designed to be CE Compliant when used in an CE compliant chassis. Maintaining CE Compliance also requires proper cabling and termination techniques. The user is advised to follow proper cabling techniques from sensor to interface to ensure a complete CE Compliant system. Industrial Computer Source does not offer engineering services for designing cabling or termination systems. Although Industrial Computer Source offers accessory cables and termination panels, it is the user's responsibility to ensure they are installed with proper shielding to maintain CE Compliance.

The PCDIO series of cards do not have any user adjustments, nor is routine maintenance required. The card is constructed with common TTL and CMOS components. The PCDIO-P family of boards come with a lifetime guarantee.

If corrective maintenance is required, contact Industrial Computer Source.

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# Appendix A - 8255 Data Sheet

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# Appendix B - Schematics

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# *Declaration of Conformity*

(according to ISO/IEC Guide 22 and EN 45014)

INDUSTRIAL COMPUTER SOURCE®

6260 Sequence Drive
San Diego, CA 92121-4371
(800) 523-2320

declares, that the product:

**PCDIO24-P PCDIO48-P PCDIO72-P PCDIO120-P PCDIO216-P**

to which this declaration relates, meets the essential health and safety requirements and is in conformity with the relevant EU Directives listed below:

**EU EMC Directive 89/336/EEC**
**EU Low Voltage Directive 72/23/EEC**

using the relevant section of the following EU standards and other normative documents:

**EN 50081-1:1992** Emissions, Generic Requirements.
-EN 55022 Measurement of radio interference charateristics of information technology equipment.

**EN 50082-2:1995** Immunity, Generic Requirements.
-EN 61000-4-2 Immunity to Electrostatic Discharge.
-ENV 50140 Immunity for radiated RF electromagnetic fields.

**EN 50082-1:1992** Immunity, Generic Requirements.
-IEC 801-3:1984 Immunity for radiated electromagnetic fields.
-IEC 801-4:1988 Immunity for AC and I/O lines, fast transient common mode.
-IEC 65A/77B Immunity for AC lines, transients, common, and differential mode.

**EN 60950:1992** Safety of Information Technology Equipment.

September 17, 1997
San Diego, CA

Mr. Steven R. Peltier
President & Chief Executive Officer

Information supporting this declaration is contained in the applicable Technical Construction file available from:

INDUSTRIAL COMPUTER SOURCE EUROPE®

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Villebon-Sur-Yvette
91961 COURTABOEUF Cedex

# BUG REPORT

While we have tried to assure this manual is error free, it is a fact of life that works of man have errors. We request you to detail any errors you find on this BUG REPORT and return it to us. We will correct the errors/problems and send you a new manual as soon as available. Please return to:

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Product: **PCDIO Series**

Manual Revision: **00431-050-27B**

Please list the page numbers and errors found. Thank you!