INDUSTRIAL COMPUTER SOURCE®

Model ISA/PCI BACKPLANE
Product Manual

MANUAL NUMBER : 00431-020-3A

INDUSTRIAL COMPUTER SOURCE®

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FOREWARD

This product manual provides information to install, operate and or program the referenced product(s) manufactured or distributed by Industrial Computer Source. The following pages contain information regarding the warranty and repair policies.

Technical assistance is available at: **1-800-480-0044**.

Manual Errors, Omissions and Bugs: A "Bug Sheet" is included as the last page of this manual. Please use the "Bug Sheet" if you experience any problems with the manual that requires correction.

Guarantee

A thirty day money-back guarantee is provided on all **standard** products sold. **Special order products** are covered by our Limited Warranty, *however they may not be returned for refund or credit. EPROMs, RAM, Flash EPROMs or other forms of solid electronic media are not returnable for credit - but for replacement only. Extended Warranty available. Consult factory.*

Refunds

In order to receive refund on a product purchase price, the product must not have been damaged by the customer or by the common carrier chosen by the customer to return the goods, and the product must be returned complete (meaning all manuals, software, cables, etc.) within 30 days of receipt and in as-new and resalable condition. The **Return Procedure** must be followed to assure prompt refund.

Restocking Charges

Product returned *after* 30 days, and *before* 90 days, of the purchase will be subject to a **minimum** 20% restocking charge and any charges for damaged or missing parts.

Products not returned within 90 days of purchase, or products which are not in as-new and re-saleable condition, are not eligible for credit return and will be returned to the customer.

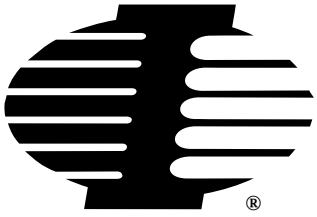
Limited Warranty

One-year limited warranty on all products sold with the exception of the "Performance Series" I/O products, which are warranted to the original purchaser for as long as they own the product, subject to all other conditions below, including those regarding neglect, misuse and acts of God. Within one year of purchase, Industrial Computer Source will repair or replace, at our option, any defective product. At any time after one year, we will repair or replace, at our option, any defective "Performance Series" I/O product sold. This does not include products damaged in shipment, or damaged through customer neglect or misuse. Industrial Computer Source will service the warranty for all standard catalog products for the first year from the date of shipment. After the first year, for products not manufactured by Industrial Computer Source, the remainder of the manufacturer's warranty, if any, will be serviced by the manufacturer directly.

The **Return Procedure** must be followed to assure repair or replacement. Industrial Computer Source will normally return your replacement or repaired item via UPS Blue. *Overnight delivery or delivery via other carriers is available at additional charge.*

The limited warranty is void if the product has been subjected to alteration, neglect, misuse, or abuse; if any repairs have been attempted by anyone other than Industrial Computer Source or its authorized agent; or if the failure is caused by accident, acts of God, or other causes beyond the control of Industrial Computer Source or the manufacturer. Neglect, misuse, and abuse shall include any installation, operation, or maintenance of the product other than in accordance with the owners' manual.

No agent, dealer, distributor, service company, or other party is authorized to change, modify, or extend the terms of this Limited Warranty in any manner whatsoever. Industrial Computer Source reserves the right to make changes or improvements in any product without incurring any obligation to similarly alter products previously purchased.



Shipments not in compliance with this Guarantee and Limited Warranty Return Policy will not be accepted by Industrial Computer Source.

Return Procedure

For any Limited Warranty or Guarantee return, please contact Industrial Computer Source's Customer Service at **1-800-480-0044** and obtain a Return Material Authorization (RMA) Number. All product(s) returned to Industrial Computer Source for service or credit **must** be accompanied by a Return Material Authorization (RMA) Number. Freight on all returned items **must** be prepaid by the customer who is responsible for any loss or damage caused by common carrier in transit. Returns for Warranty **must** include a Failure Report for each unit, by serial number(s), as well as a copy of the original invoice showing date of purchase.

> To reduce risk of damage, returns of product must be in an Industrial Computer Source shipping container. If the original container has been lost or damaged, new shipping containers may be obtained from Industrial Computer Source Customer Service at a nominal cost.

Limitation of Liability

In no event shall Industrial Computer Source be liable for any defect in hardware or software or loss or inadequacy of data of any kind, or for any direct, indirect, incidental, or consequential damages in connection with or arising out of the performance or use of any product furnished hereunder. Industrial Computer Source liability shall in no event exceed the purchase price of the product purchased hereunder. The foregoing limitation of liability shall be equally applicable to any service provided by Industrial Computer Source or its authorized agent.

Some *Sales Items* and *Customized Systems* are **not** subject to the guarantee and limited warranty. However, in these instances any deviations will be disclosed prior to sales and noted in the original invoice. ***Industrial Computer Source reserves the right to refuse returns or credits on software or special order items.***

Advisories

Three types of advisories are used throughout the manual to stress important points or warn of potential hazards to the user or the system. They are the Note, the Caution, and the Warning. Following is an example of each type of advisory:

Note: The note is used to present special instruction, or to provide extra information which may help to simplify the use of the product.

CAUTION!

A Caution is used to alert you to a situation which if ignored may cause injury or damage equipment.

WARNING!

A Warning is used to alert you of a situation which if ignored will cause serious injury.

Cautions and Warnings are accented with triangular symbols. The exclamation symbol is used in all cautions and warnings to help alert you to the important instructions. The lightning flash symbol is used on the left hand side of a caution or a warning if the advisory relates to the presence of voltage which may be of sufficient magnitude to cause electrical shock.

Use caution when servicing any electrical component. We have tried to identify the areas which may pose a Caution or Warning condition in this manual; however, Industrial Computer Source does not claim to have covered all situations which might require the use of a Caution or Warning.

You must refer to the documentation for any component you install into a computer system to insure proper precautions and procedures are followed.

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Current Revision 3A

July 1997

Chapter 1: Introduction

Features

- 6 layer printed circuit board
- Extremely high EMI and RFI noise immunity
- Accept power connectors from standard PC bus power supplies
- Accepts CPU's with PCI Local Bus Extensions and standard ISA Bus CPU's
- Bus Power Check™ LED indicators for +3.3, +5, -5, +12, -12 VDC supplies
- Allows use of standard ISA Bus and PCI Local Bus option cards
- Bus terminating resistor sockets

Industrial Computer Source passive ISA/PCI backplanes are manufactured to the highest standards. They provide PCI Local Bus and ISA bus archietures to provide maximum flexibility in upgrage decisions. A standard ISA CPU may be installed in any ISA slot. A CPU with the PICMG compliant PCI Local Bus extension connector, installed in the ISA/PCI CPU slot, will provide full use of the PCI and ISA bus.

The DEC 21152 PCI-to-PCI bridge chip is incorporated into the design of the backplanes to overcome the PCI load limitations. The bridge chip adds a secondary PCI bus which operates independantly from the primary PCI bus, actually increasing overall performace in certain applications.

The backplane configurations are as follows:

15005-02	2/1/2	Two ISA slots, one dedicated ISA/PCI CPU slot, and two PCI slots.
15008-02	3/1/4	Three ISA slots, one dedicated ISA/PCI CPU slot, and four PCI slots. One of the PCI slots is located on the Primary PCI bus and the other three are located on the secondary PCI Bus.
14008-02	5/1/2	Five ISA slots, one dedicated ISA/PCI CPU slot, and two PCI slots.
15013-02	6/1/6	Six ISA slots, one dedicated ISA/PCI CPU slot, and six PCI slots. Two of the PCI slots are located on the Primary PCI bus and four are located on the secondary PCI Bus.
14013-10	10/1/2	Ten ISA slots, one dedicated ISA/PCI CPU slot, and two PCI slots.
15018-02	8/1/9	Eight ISA slots, one dedicated ISA/PCI CPU slot, and nine PCI slots. One of the PCI slots is located on the Primary PCI bus, four are located on the secondary PCI Bus, and four more are located on an additional secondary bus.
15018-10	11/1/6	Eleven ISA slots, one dedicated ISA/PCI CPU slot, and six PCI slots. One of the PCI slots is located on the Primary PCI bus, four are located on the secondary PCI Bus, and four more are located on an additional secondary bus PCI.

Each backplane is of a low capacitance design. This design minimizes signal crosstalk while keeping trace capacitance low which improves signal edges and rise and fall times. Each backplane also has a bank of LEDs to indicate the presence of the various power supply levels of the standard PC bus - ±5VDC, ±12VDC, and +3.3VDC. These LEDs provide a quick check of power supply operation without the need of a multimeter.

The Industrial Computer Source passive backplanes have been tested with a variety of plug-in CPU cards, from 8088 XT through Pentium and DEC Alpha systems. For applications involving option cards that are sensitive to bus impedance, termination SIPs are available as plug-ins to terminate the ISA bus of the backplane. Please refer to the section on Bus Termination for more detailed information.

CAUTION!

Not all PCI cards work in all PCI slots in bridged backplanes. Some video cards cause bus contention when placed in certain PCI slots. This will cause fatal bus errors and potential damage to parts due to overheating. This problem can be avoided by placing your video card in Slot 2 for the 15013-02 backplane or Slot 1 on the 15008-02, 15018-2 backplanes, and 15018-10. Note that video cards that are PCI 2.1 compliant will not cause problems in a bridge chip environment.

Backplane Construction

The ISA/PCI backplanes are constructed of 6 layers, with internal ground and power planes for RFI and EMI noise immunity and low trace capacitance. The signal traces are located on the outer layers (layers 1 and 6) and the inner layers (layers 3 and 4). The inner signal layers are used for clock and control signals. Layer 2 is the Ground plane and layer 5 is the Power plane.

Connectors

Each backplane provides a 16-pin Molex-type connector for power input. A variety of auxiliary power and sense connectors are also provided for various chassis functions. Please see the Dimensional Drawings for pin assignments and orientations.

Input Power

Each input is filtered by one or more large electrolytic capacitors for low frequency line noise rejection. Ceramic bypass filter capacitors of 0.01µF improve noise immunity. All five input voltages have bypass capacitors.

Each power supply output is monitored by the exclusive Industrial Computer Source Bus Power Check™ circuitry. A separate LED is lit by each supply voltage for a quick visible check of power supply operation. This is not, however, a tolerance verification. Troubleshooting requirements may require actual measurement of the power supply values to ensure operation to specified limits.

Note that troubleshooting a chassis may require a load on the power supply. Industrial Computer Source offers an optional ISA plug-in Power Supply Load Board that provides the minimum loading requirements of 0.96A load on +12VDC and 4A load on +5VDC. Please mention Model 10273-01B when ordering.

ISA BUS Termination

Termination works as an impedance mismatch at the end of the bus, minimizing or preventing reflections and interference. If there is no termination, signals reach the end of the bus and reflect back down the bus. In extreme cases, the reflected signals can interfere with the real bus information, leading to spurious operation or lockups. This can become a significant factor as bus lengths and speeds increase. The applications most likely to be affected are telephony or other applications with many I/O boards drawing high current values off the +12V or -12V power connections.

Industrial Computer Source backplanes have supported 166MHz systems without bus termination and without problem. However, provision is made for installing terminations that might be required for your application.

Terminations connect the bus to +5VDC and ground, providing a path for the bus signals to dissipate. A terminated bus provides signals with less noise, although rise and fall times are slower. However, results are dependent on the CPU and option cards being used, and must be evaluated on a case-by-case basis.

There are three types of terminations that may be used; A Resistor Network; an RC Network; or a Diode Termination. A Resistor Network will provide the required impedance mismatch, but does result in loading. A RC Network does not impose a static load as a Resistor Network will, but it will affect the timing factors of the line to some degree. A Diode Termination is generally used in conjunction with a Resistor Network to reduce over- and under-shoot.

All Pentium and 486 vesa local or PCI CPU control signals that should never be terminated are as follows:

A-1 (RES 12-3)	I/OCHCK
B-8 (RES 12-7)	0WS
D-1 (RES 6-8)	MEMCS16
D-2 (RES 6-9)	I/0CS16
D-17 (RES 4-9)	MASTER

To end termination of a signal, simply cut the wire on the terminating resistor for the appropriate signal.

The backplanes provide termination sockets at the left end of the bus. These sockets accept standard 10-position SIPS manufactured by Bournes and others. Not all signal lines are available for termination. Refer to page 2-6 for the BUS signal information.

Resistor Termination

The goal of termination resistors is to provide an impedance mismatch at the end of the bus to prevent signal reflections. This mismatch has to be balanced by the electrical capability of the CPU and option cards to drive the load imposed by the resistors.

Generally, terminations that connect to both +5V and ground work best, although terminations to +5V only are allowable.

One way to provide terminations in digital systems is a resistor network connected to both +5V and ground. The following two examples represent such a resistor network in Single Inline Pin (SIP) form. Note that in both examples, the SIPs are inserted with pin 1 of the SIP toward the back of the chassis. While the following examples specify Bourns part numbers, equivalent values from other manufactures may be used. The following provides 330 ohms to +5V and 220 ohms to ground.

- Bourns part # 4610X-104-221/331 (Low profile)
- Bourns part # 4610M-104-221/331 (Medium profile)

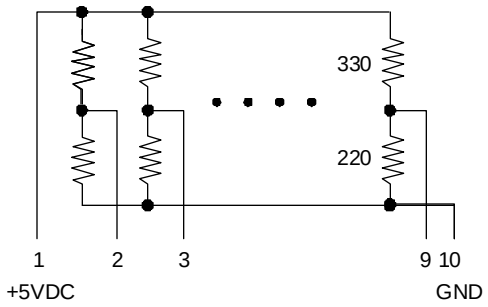

Figure 1-1: Resistor SIP Network

Reading the resistance from the signal pin of the SIP to either pin 1 or pin 10 will not provide the expected resistance of, for example, 220 or 330 ohms. This is because of the parallel resistance of the other paths. For example, the 220 ohms side will read 143 ohms (pin 10), and the 330 ohms side will read 156 ohms (pin 1). The actual values will change slightly because of allowed tolerance.

The following combination provides less bus loading than the first example and provides 330 ohms to +5 and 470 ohms to ground:

- Bourns part # 4610X-104-331/471 (Low profile)
- Bourns part # 4610M-104-331/471 (Medium profile)

Other values are manufactured and can certainly be used if a problem persists on the bus. Not all cards behave well on large buses or in combination with other cards and may require some experimentation to completely isolate all intermittent operation. Turning the SIP around is allowed, even recommended occasionally, to better shape the signal being pulled high.

RC Network Termination

An alternative to a resistor network is an RC network. An RC network connects the signal lines through a resistor in series with a capacitor, to either +5V or ground. An advantage of an RC Network is that no static load is imposed on the bus, but increased capacitance on the line will affect timing factors. RC Networks are also slightly more expensive than Resistor Networks.

DIODE Termination

In some cases, diodes can be connected between the signal lines and both +5V and ground. Any spikes greater than the +5V rail are shunted and limited to +5V. Any negative spikes are shunted to ground. Thus, the bus sees only signals in the range of 0-5V. Diode termination reduces over- and under-shoot, but doesn't improve signal shape or edge times. Diode termination is generally used in conjunction with resistor termination.

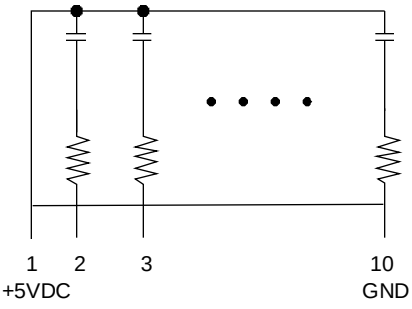

Figure 1-2: RC SIP Network

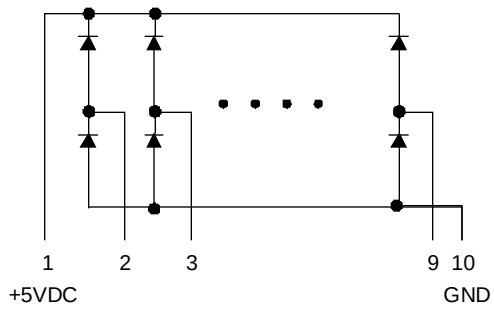

Figure 1-3: Diode SIP Network

Connectors

5 Slot Backplane, 15005-02

P2 - Drive Power Out Connector

4 pin single row, Amp 640457-4

1	+12VDC
2	GND
3	GND
4	+5VDC

P3 - Drive Power Out Connector

4 pin single row, Amp 640457-4

1	+12VDC
2	GND
3	GND
4	+5VDC

P7- CPU Connector

8 pin single row, Amp 640457-8

1	SPKDATA
2	N/C
3	KBDLOCK
4	KBDDAT
5	KBDCLK
6	N/C
7	GND
8	RESET

P8/P9 - Power Supply Connector

16 pin single row, Amp 1-640445-6

1	N/C	(P8)
2	N/C	(P8)
3	+12V	(P8)
4	-12V	(P8)
5	GND	(P8)
6	GND	(P8)
7	GND	
8	GND	
9	GND	(P9)
10	GND	(P9)
11	-5V	(P9)
12	+5V	(P9)
13	+5V	(P9)
14	+5V	(P9)
15	+5V	
16	+5V	

P10 - 5 Volt Power Connector

Unused: Not Populated

This connector is disabled on this board and should not be used.

P11 - 3.3 Volt Power Connector

6 pin single row, Amp 640445-6

1	+3.3V
2	+3.3V
3	+3.3V
4	GND
5	GND
6	GND

P12 - Connection to CPU

10 pin single row, Amp 1-640457-0

1	-12V
2	+12V
3	SPKDATA
4	+5V
5	KBDLOCK
6	KBDDAT
7	KBDCLK
8	-5V
9	GND
10	RESET
11	GND
12	+3.3V

8 Slot Backplane, 15008-02 and 14008-02

P1 - I/O Power Out

3 pin single row, Amp 640457-3

1 +5VDC
2 +12VDC
3 GND

P3 - Drive Power Out Connector

4 pin single row, Amp 640457-4

1 +12VDC
2 GND
3 GND
4 +5VDC

P5- I/O Power Out Connector

2 pin single row, Amp 640475-2

1 +5VDC
2 GND

P7- CPU Connector

8 pin single row, Amp 640457-8

1 SPKDATA
2 N/C
3 KBDLOCK
4 KBDDAT
5 KBDCLK
6 N/C
7 GND
8 RESET

P8/P9 - Power Supply Connector

16 pin single row, Amp 1-640445-6

1 N/C (P8)
2 N/C (P8)
3 +12V (P8)
4 -12V (P8)
5 GND (P8)
6 GND (P8)
7 GND
8 GND
9 GND (P9)
10 GND (P9)
11 -5V (P9)
12 +5V (P9)
13 +5V (P9)
14 +5V (P9)
15 +5V
16 +5V

P10 - 5 Volt Power Connector

6 pin single row, Amp 640445-6

1 +5V
2 +5V
3 +5V
4 GND
5 GND
6 GND

P11 - 3.3 Volt Power Connector

6 pin single row, Amp 640445-6

1 +3.3V
2 +3.3V
3 +3.3V
4 GND
5 GND
6 GND

P12 - Connection to CPU

10 pin single row, Amp 1-640457-0

1	-12V
2	+12V
3	SPKDATA
4	+5V
5	KBDLOCK
6	KBDDAT
7	KBDCLK
8	-5V
9	GND
10	RESET
11	GND
12	+3.3V

13 Slot Backplane, 15013-02 and 14013-02

P1 - I/O Power Out

3 pin single row, Amp 640457-3

1 +5VDC
2 +12VDC
3 GND

P2 - Drive Power Out Connector

4 pin single row, Amp 640389-4

1 +12VDC
2 GND
3 GND
4 +5VDC

P3 - Drive Power Out Connector

4 pin single row, Amp 640457-4

1 +12VDC
2 GND
3 GND
4 +5VDC

P4 - I/O Power Out

3 pin single row, Amp 640389-3

1 +5VDC
2 +12VDC
3 GND

P5- I/O Power Out Connector

2 pin single row, Amp 640457-2

1 +5VDC
2 GND

P6 - I/O Power Out

3 pin single row, Amp 640389-3

1 +5VDC
2 +12VDC
3 GND

P7- CPU Connector

8 pin single row, Amp 640457-8

1 SPKDATA
2 N/C
3 KBDLOCK
4 KBDDAT
5 KBDCLK
6 N/C
7 GND
8 RESET

P8/P9 - Power Supply Connector

16 pin single row, Amp 1-640445-6

1 N/C (P8)
2 N/C (P8)
3 +12V (P8)
4 -12V (P8)
5 GND (P8)
6 GND (P8)
7 GND
8 GND
9 GND (P9)
10 GND (P9)
11 -5V (P9)
12 +5V (P9)
13 +5V (P9)
14 +5V (P9)
15 +5V
16 +5V

P10 - 5 Volt Power Connector

6 pin single row, Amp 640445-6

1 +5V
2 +5V
3 +5V
4 GND
5 GND
6 GND

P11 - 3.3 Volt Power Connector

6 pin single row, Amp 640445-6

1	+3.3V
2	+3.3V
3	+3.3V
4	GND
5	GND
6	GND

P12 - Connection to CPU

10 pin single row, Amp 1-640456-0

1	-12V
2	+12V
3	SPKDATA
4	+5V
5	KBDLOCK
6	KBDDAT
7	KBDCLK
8	-5V
9	GND
10	RESET
11	GND
12	+3.3V

18 Slot Backplane, 15018-02 and 15018-10

P1- Remote Sense Connector

2 pin single row, Amp 640457-2

1 +5VDC
2 GND

P2 - Connection to CPU

10 pin single row, Amp 1-640457-0

1 -12V
2 +12V
3 SPKDATA
4 +5V
5 KBDLOCK
6 KBDDAT
7 KBDCLK
8 -5V
9 GND
10 RESET
11 GND
12 +3.3V

P3- Remote Sense Connector

2 pin single row, Amp 640457-2

1 +5VDC
2 GND

P4 - I/O Power Out

3 pin single row, Amp 640457-3

1 +5VDC
2 +12VDC
3 GND

P5- Auxilary CPU Connector

8 pin single row, Amp 640457-8

1 SPKDATA
2 N/C
3 KBDLOCK
4 KBDDAT
5 KBDCLK
6 N/C

P5- Auxilary CPU Connector (cont)

7 GND
8 RESET

P6 - Drive Power Out Connector

4 pin single row, Amp 640389-4

1 +12VDC
2 GND
3 GND
4 +5VDC

P7 - Drive Power Out Connector

4 pin single row, Amp 640389-4

1 +12VDC
2 GND
3 GND
4 +5VDC

P8 - I/O Power Out

3 pin single row, Amp 640389-3

1 +5VDC
2 +12VDC
3 GND

P9 - Power Supply Connector

16 pin single row, Amp 1-640389-6

1	N/C	(P8)
2	N/C	(P8)
3	+12V	(P8)
4	-12V	(P8)
5	GND	(P8)
6	GND	(P8)
7	GND	
8	GND	
9	GND	(P9)
10	GND	(P9)
11	-5V	(P9)
12	+5V	(P9)
13	+5V	(P9)
14	+5V	(P9)
15	+5V	
16	+5V	

P10 - Power Supply Connector

6 pin single row, Amp 640389-6

1	-12V
2	GND
3	GND
4	-5V
5	+12V
6	+5V

P11 - I/O Power Out

3 pin single row, Amp 640389-3

1	+5VDC
2	+12VDC
3	GND

P12 - 5 Volt Power Connector

6 pin single row, Amp 640389-6

1	+5V
2	+5V
3	+5V
4	GND
5	GND
6	GND

P13 - 3.3 Volt Power Connector

6 pin single row, Amp 640445-6

1	+3.3V
2	+3.3V
3	+3.3V
4	GND
5	GND
6	GND

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Chapter 2: ISA Bus Overview

ISA Bus Signal Descriptions

The following is a description of the ISA Bus signals. All signal lines are TTL-compatible. A # symbol at the end of a signal name indicates that the active state occurs when the signal is at a low voltage. When the # symbol is absent, the signal is active at a high voltage.

AEN — Address Enable is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active, the DMA controller has control of the address bus, the data-bus Read command lines (memory and I/O), and the Write command lines (memory and I/O).

BALE — Address Latch Enable (BALE) is provided by the bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. It is available to the I/O channel as an indicator of a valid microprocessor or DMA address (when used with AEN). Microprocessor addresses SA[19..0] are latched with the falling edge of BALE. BALE is forced high during DMA cycles.

CLK — CLK is the system clock. The clock has a 50% duty cycle. This signal should only be used for synchronization. It is not intended for uses requiring a fixed frequency.

DACK[7..5]#, DACK[3..0]# — DMA Acknowledge DACK[7..5]# and DACK[3..0]# are used to acknowledge DMA requests DRQ[7..5] and DRQ[3..0]. They are active low.

DRQ[7..5], DRQ[3..0] — DMA Requests DRQ[7..5] and DRQ[3..0] are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). They are prioritized, with DRQ0 having the highest priority and DRQ7 having the lowest. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding DMA Request Acknowledge (DACK) line goes active. DRQ[3..0] will perform 8-bit DMA transfers; DRQ[7..5] will perform 16-bit transfers.

I/O CHRDY — I/O Channel Ready is pulled low by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of clock cycles. This signal should be held low for no more than 2.5 microseconds.

IOCHK# — I/O Channel Check provides the system board with parity information about memory or devices on the I/O channel. When this signal is active, it indicates an uncorrectable system error.

IOCS16# — I/O 16 Chip Select signals the system board that the present data transfer is a 16-bit, 1 wait-state, I/O cycle. It is derived from an address decode. IOCS16# is active low and should be driven with an open collector or tri-state driver capable of sinking 20mA.

IOR# I/O Read instructs an I/O device to read the data in the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is active low.

IOW# I/O Write instructs an I/O device to drive its data onto the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is active low.

IRQ[15,14], IRQ[12..9], IRQ[7..3]

Interrupt Requests are used to signal the microprocessor that an I/O device needs attention. The interrupt requests are prioritized, with IRQ[15..14] and IRQ[12..9] having the highest priority (IRQ9 is the highest) and IRQ[7..3] having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine).

LA[23..17] These signals (unlatched) are used to address memory and I/O devices within the system. They give the system up to 16MB of addressability. These signals are valid when BALE is high. LA[23..17] are not latched during microprocessor cycles and therefore do not stay valid for the whole cycle. Their purpose is to generate memory decodes for 1 wait-state memory cycles. These decodes should be latched by I/O adapters on the falling edge of BALE. These signals also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

Master# Master# is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a DACK#. Upon receiving the DACK#, an I/O microprocessor may pull Master# low, which will allow it to control the system address, data, and control lines (a condition known as tri-state). After Master# is low, the I/O microprocessor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15 microseconds, system memory may be lost because of a lack of refresh.

MEMCS16# M16# Chip Select signals the system board if the present data transfer is a 1 wait-state, 16-bit, memory cycle. It must be derived from the decode of LA[23..17]. MEMCS16# should be driven with an open collector or tri-state driver capable of sinking 20mA.

0WS# The Zero Wait State (0WS#) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, 0WS# is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8-bit device with a minimum of two wait states, 0WS# should be driven active on system clock after the Read or Write command is active gated with the address decode for the device. Memory Read and Write commands to a 8-bit device are active on the falling edge of the system clock. 0WS# is active low and should be driven with an open collector or tri-state driver capable of sinking 20mA.

OSC Oscillator (OSC) is a high-speed clock with a 70-nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle.

REFRESH# The REFRESH# signal is used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel.

RESET Reset is used to reset or initialize system logic at power-up time or during a low line-voltage outage. This signal is active high.

SA[19..0] Address bits SA[19..0] are used to address memory and I/O devices within the system. These twenty address lines, in addition to LA[23..17], allow access of up to 16MB of memory. SA[19..0] are gated on the system bus when BALE is high and are latched in the falling edge of BALE. These signals are generated by the microprocessors or DMA Controller. They also may be driven by other microprocessors or DMA controllers that reside in the I/O channel.

SBHE# System Bus High Enable (SBHE#) indicates a transfer of data on the upper byte of the data bus, SD[15..8]. 16-bit devices use SBHE# to condition data bus buffers tied to SD[15..8].

SD[15..0] Data signals SD[15..0] provide bus bits 15 through 0 for the microprocessor, memory, and I/O devices. SD15 is the most-significant bit and SD0 is the least-significant bit. All 8-bit devices on the I/O channel should use SD[7..0] for communications to the microprocessor. The 16-bit devices will use SD[15..0]. To support 8-bit devices, the data on SD[15..8] will be gated to SD[7..0] during 8-bit transfers to these devices. 16-bit microprocessor transfers to 8-bit devices will be converted to two 8-bit transfers.

SMEMR#, MRMR#

These signals instruct the memory devices to drive data onto the data bus. SMEMR# is active only when the memory decode is within the low 1MB of memory space. MRMR# is active on all memory read cycles. MRMR# may be driven by any microprocessor or DMA controller in the system. SMEMR# is derived from MRMR# and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive MRMR#, it must have the address lines valid on the bus for one system clock period before driving MRMR# active. Both signals are active low.

SMEMW#, MEMW#

These signals instruct the memory devices to store the data present on the data bus. SMEMW# is active only when the memory decode is within the low 1MB of the memory space. MEMW# is active on all memory write cycles. MEMW# may be driven by any microprocessor or DMA controller in the system. SMEMW# is derived from MEMW# and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive MEMW#, it must have the address lines valid on the bus for one system clock period before driving MEMW# active. Both signals are active low.

T/C Terminal Count (T/C) provides a pulse when the terminal count for any DMA channel is reached.

XT (8 BIT) Bus Pin Assignments

Solder Side of Option Board			
Description	**Res**	**Pin**	**Side**
Ground	NC	1	B
Reset	4.7K	2	B
+5 Volts	NC	3	B
IRQ2 or 9	NC	4	B
-5 Volts	NC	5	B
DRQ2	NC	6	B
-12 Volts	NC	7	B
0WS#	12-7	8	B
+12 Volts	NC	9	B
Ground	NC	10	B
SMEMW#	9-2	11	B
SMEMR#	9-3	12	B
IOW#	9-4	13	B
IOR#	9-5	14	B
DACK3#	9-6	15	B
DRQ3	NC	16	B
DACK1#	9-7	17	B
DRQ1	NC	18	B
REFRESH#	9-8	19	B
CLK	9-9	20	B
IRQ7	NC	21	B
IRQ6	NC	22	B
IRQ5	NC	23	B
IRQ4	NC	24	B
IRQ3	NC	25	B
DACK2#	6-2	26	B
T/C	6-3	27	B
BALE	6-4	28	B
+5 Volts	NC	29	B
OSC	6-5	30	B
Ground	NC	31	B

Component side of Option Board			
Side	**Pin**	**Res**	**Description**
A	1	12-2	I/OCHK#
A	2	11-2	SD7
A	3	11-3	SD6
A	4	11-4	SD5
A	5	11-5	SD4
A	6	11-6	SD3
A	7	11-7	SD2
A	8	11-8	SD1
A	9	11-9	SD0
A	10	NC	I/OCHRDY
A	11	12-9	AEN
A	12	10-6	SA19
A	13	10-7	SA18
A	14	10-8	SA17
A	15	10-9	SA16
A	16	8-2	SA15
A	17	8-3	SA14
A	18	8-4	SA13
A	19	8-5	SA12
A	20	8-6	SA11
A	21	8-7	SA10
A	22	8-8	SA9
A	23	8-9	SA8
A	24	7-2	SA7
A	25	7-3	SA6
A	26	7-4	SA5
A	27	7-5	SA4
A	28	7-6	SA3
A	29	7-7	SA2
A	30	7-8	SA1
A	31	7-9	SA0

Note: Pin B4 is IRQ2 for an XT

Pin B4 is IRQ9 for an AT which is redirected as IRQ2

* -REFRESH is -DACK0 on an XT 8-bit system.

AT (16 BIT) Bus Extension Pin Assignments

Solder Side of Option Board			
Description	**Res**	**Pin**	**Side**
MEMCS16#	6-8	1	D
I/OCS16#	6-9	2	D
IRQ10	NC	3	D
IRQ11	NC	4	D
IRQ12	NC	5	D
IRQ15	NC	6	D
IRQ14	NC	7	D
DACK0#	4-2	8	D
DRQ0#	NC	9	D
DACK5#	4-5	10	D
DRQ5	NC	11	D
DACK6#	4-7	12	D
DRQ6#	NC	13	D
DACK7#	4-8	14	D
DRQ7	NC	15	D
5VDC	NC	16	D
MASTER#	4-9	17	D
GROUND	NC	18	D

Component Side of Option Board			
Side	**Pin**	**Res**	**Description**
C	1	6-7	SBHE#
C	2	5-3	LA23
C	3	5-4	LA22
C	4	5-5	LA21
C	5	5-6	LA20
C	6	5-7	LA19
C	7	5-8	LA18
C	8	5-9	LA17
C	9	4-4	MRMR#
C	10	4-6	MEMW#
C	11	3-2	SD08
C	12	3-3	SD09
C	13	3-4	SD10
C	14	3-5	SD11
C	15	3-6	SD12
C	16	3-7	SD13
C	17	3-8	SD14
C	18	3-9	SD15

BUS Signals sorted by SIP Resistors

Side	Pin	Res/Pin	Description
		RN3-1	+5V
C	11	RN3-2	SD08
C	12	RN3-3	SD09
C	13	RN3-4	SD10
C	14	RN3-5	SD11
C	15	RN3-6	SD12
C	16	RN3-7	SD13
C	17	RN3-8	SD14
C	18	RN3-9	SD15
		RN3-10	GND
		RN4-1	+5V
D	8	RN4-2	DACK0#
		RN4-3	NC
C	9	RN4-4	MRMC#
D	10	RN4-5	DACK5#
C	10	RN4-6	MEMW#
D	12	RN4-7	DACK6#
D	14	RN4-8	DACK7#
D	17	RN4-9	MASTER#
		RN4-10	GND
		RN5-1	+5V
		RN5-2	NC
C	2	RN5-3	LA23
C	3	RN5-4	LA22
C	4	RN5-5	LA21
C	5	RN5-6	LA20
C	6	RN5-7	LA19
C	7	RN5-8	LA18
C	8	RN5-9	LA17
		RN5-10	GND

Side	Pin	Res/Pin	Description
		RN6-1	+5V
B	26	RN6-2	DACK2#
B	27	RN6-3	T-C
B	28	RN6-4	BALE
B	30	RN6-5	OSC
		RN6-6	NC
C	1	RN6-7	SBHE#
D	1	RN6-8	MEMCS16#
D	2	RN6-9	I/O16#
		RN6-10	GND
		RN7-1	+5V
A	24	RN7-2	SA7
A	25	RN7-3	SA6
A	26	RN7-4	SA5
A	27	RN7-5	SA4
A	28	RN7-6	SA3
A	29	RN7-7	SA2
A	30	RN7-8	SA1
A	31	RN7-9	SA0
		RN7-10	GND
		RN8-1	+5V
A	16	RN8-2	SA15
A	17	RN8-3	SA14
A	18	RN8-4	SA13
A	19	RN8-5	SA12
A	20	RN8-6	SA11
A	21	RN8-7	SA10
A	22	RN8-8	SA9
A	23	RN8-9	SA8
		RN8-10	GND

BUS Signals sorted by SIP Resistors (cont)

Side	Pin	Res/Pin	Description
		RN9-1	+5V
B	11	RN9-2	SMEMW#
B	12	RN9-3	SMEMR#
B	13	RN9-4	IOW#
B	14	RN9-5	IOR#
B	15	RN9-6	DACK3#
B	17	RN9-7	DACK1#
B	19	RN9-8	REFRESH#
B	20	RN9-9	CLK
		RN9-10	GND
		RN10-1	+5V
		RN10-2	NC
		RN10-3	NC
		RN10-4	NC
		RN10-5	NC
A	12	RN10-6	SA19
A	13	RN10-7	SA18
A	14	RN10-8	SA17
A	15	RN10-9	SA16
		RN10-1	GND

Side	Pin	Res/Pin	Description
		RN11-1	+5V
A	2	RN11-2	SD7
A	3	RN11-3	SD6
A	4	RN11-4	SD5
A	5	RN11-5	SD4
A	6	RN11-6	SD3
A	7	RN11-7	SD2
A	8	RN11-8	SD1
A	9	RN11-9	SD0
		RN11-10	GND
		RN12-1	+5V
A	1	RN12-2	I/OCHK#
		RN12-3	NC
		RN12-4	NC
		RN12-5	NC
		RN12-6	NC
B	8	RN12-7	0WS#
		RN12-8	NC
A	11	RN12-9	AEN
		RN12-10	GND

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Chapter 3: PCI Bus Overview

The PCI Local Bus is a high performance, 32-bit or 64-bit bus with multiplexed address and data lines. It is intended for use as an interconnect mechanism between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems.

The PCI component and add-in card interface is processor independent, enabling an efficient transition to future processor architectures. Processor independence allows the PCI Local Bus to be optimized for I/O functions, enables concurrent operation of the local bus with the processor/memory subsystem, and accommodates high performance peripherals in addition to graphics. Movement to enhanced video and multimedia displays and other high bandwidth I/O will continue to increase local bus bandwidth requirements. A transparent 64-bit extension of the 32-bit data and address buses is defined, doubling the bus bandwidth and offering forward and backwards compatibility of 32-bit and 64-bit PCI Local Bus peripherals.

The PCI Local Bus standard offers additional benefits to the users of PCI based systems. Configuration registers are specified for PCI components and add-in cards. A system with embedded auto configuration software offers true ease-of-use for the system user by automatically configuring PCI add-in cards at power on.

DEC Bridge Chip

The DEC bridge chip is a high-performance chip that expands the electrical capacity of all PCI systems. The bridge chip allows more PCI devices than a single PCI bus can support. The bridge chip has two PCI interfaces. The primary PCI interface connects directly to the PCI bus closest to the host CPU. The secondary PCI interface creates a new and independent PCI bus. The primary function of the bridge is to allow transactions to occur between a master on one PCI bus and a target on the other PCI bus.

The bridge chip also allows the two PCI buses to operate independently. A master and a target located on the same PCI bus can communicate with each other even if the other PCI bus is busy. As a result, the bridge can isolate traffic between devices on one PCI bus from devices on other PCI buses. This is a major benefit to system performance in some applications such as multimedia.

The bridge chip can extend a system beyond the electrical loading limits of a single PCI bus. Each new PCI bus created by the addition of a bridge chip provides support for additional electrical loads.

PCI Signal Definitions

The PCI interface requires a minimum of 47 pins for a target-only device and 49 pins for a master to handle data and addressing, interface control, arbitration, and system functions. Figure 2-1 shows the pins in functional groups, with required pins on the left side and optional pins on the right side. The direction indicator on signals in Figure 2-1 assumes a combination master/target device.

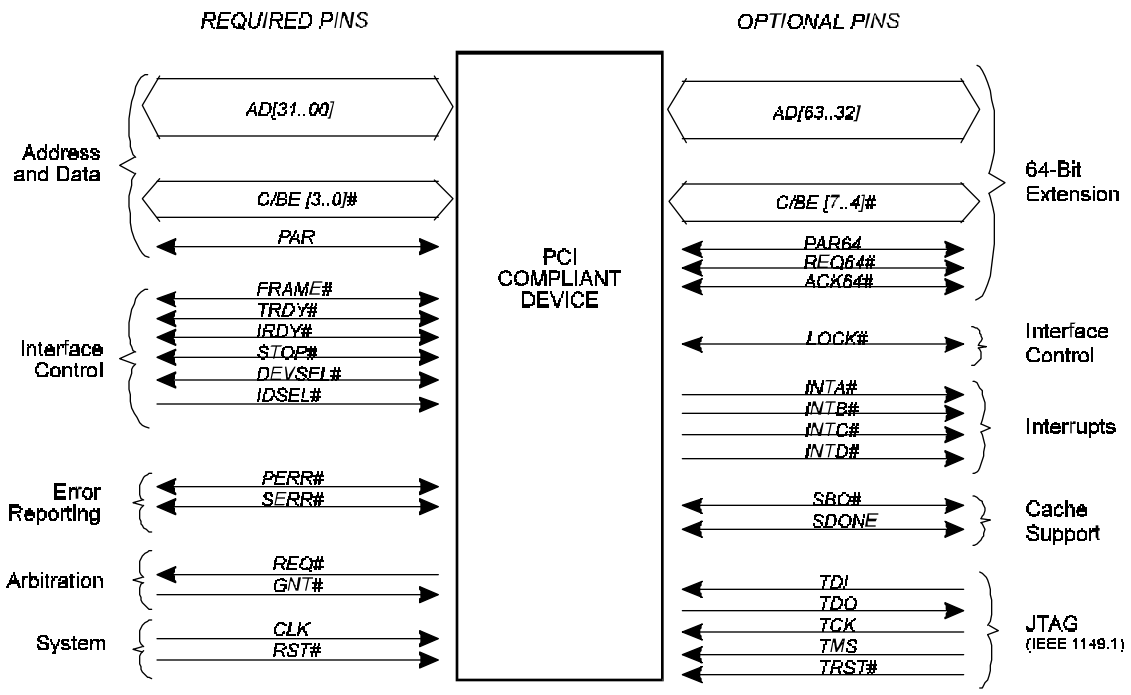

Figure 2-1: PCI Signals

Pin Functional Groups

The PCI pin definitions are organized in the functional groups shown in Figure 2-1. A # symbol at the end of a signal name indicates that the active state occurs when the signal is at a low voltage. When the # symbol is absent, the signal is active at a high voltage.

System Pins

CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device.
RST#	Reset is used to bring PCI specific registers, sequencers, and signals to a consistent state.

Address and Data Pins

AD[31..00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts.
C/BE [3..0]#	Bus Commands and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, these pins define the bus command; during the data phase they are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE0# applies to byte 0 (lsb) and C/BE3# applies to byte 3 (msb).

PAR — Parity is even parity across AD[31..00] and C/BE[3..0]#. Parity generation is required by all PCI agents. The master drives PAR for address and write data phases; the target drives PAR for read data phases.

Interface Control Pins

FRAME# — Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase.

IRDY# — Initiator Ready indicates the agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRD#. A data phase is completed on any clock that both IRDY# and TRDY# are sampled asserted. Wait cycles are inserted until both signals are asserted together.

TRDY# — Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRD#. A data phase is completed on any clock that both IRDY# and TRDY# are sampled asserted. Wait cycles are inserted until both signals are asserted together.

STOP# — Stop indicates the current target is requesting the master to stop the current transaction.

LOCK# — Lock indicates an operation may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#.

IDSEL — Initialization Device Select is used as a chip select during configuration read and write transactions.

DEVSEL# — Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

Arbitration Pins (Bus Masters only)

REQ# — Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ#.

GNT# — Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT#.

Error Reporting Pins

PERR# — Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. PERR# is sustained tri-state and must be driven active by the agent receiving data when a data parity error is detected.

SERR# System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt to be generated, a different reporting mechanism is required.

Interrupt Pins (Optional)

Interrupts on PCI are optional and defined as level sensitive, asserted low (negative true), using open drain output drivers. PCI defines one interrupt for a single function and up to four interrupt lines for a multifunction device or connector.

INTA# INTA# is used to request an interrupt. For a single function device, only INTA# may be used, while the other three interrupt lines have no meaning.

INTB#, INTC#, INTD#

These interrupts are used to request additional interrupts and only have meaning on a multifunction device.

Cache Support Pins (Optional)

A cacheable PCI memory should implement both cache support pins as inputs, to allow it to work with either write-through or write-back caches.

SBO# Snoop Backoff indicates a hit to a modified line when asserted. When SBO# is deasserted and SDONE is asserted it indicates a clean snoop result.

SDONE Snoop Done indicates the status of the snoop for the current access. When deasserted, it indicates the result of the snoop is still pending. When asserted, it indicates the snoop is complete.

64-Bit Bus Extension Pins (Optional)

The 64-bit extension pins are collectively optional. That is, if the 64-bit extension is used, all the pins in this section are required.

AD[63..32] Address and Data are multiplexed in the same pins and provide 32 additional bits. During an address phase, the upper 32-bits of a 64-bit address are transferred. During a data phase, an additional 32-bits of data are transferred when REQ64# and ACK64# are both asserted.

C/BE[7..4]# Bus Command and Byte Enables are multiplexed on the same pins. During an address phase, the actual bus command is transferred. During a data phase, they are byte enables indicating which byte lanes carry meaningful data when REQ64# and ACK64# are both asserted.

REQ64# Request 64-bit Transfer, when actively driven by the current bus master, indicates it desires to transfer data using 64 bits.

ACK64#	Acknowledge 64-bit Transfer, when actively driven by the device that has positively decoded its address as the target of the current access, indicates the target is willing to transfer data using 64 bits.
PAR64	Parity Upper DWORD is the even parity bit that protects AD[63..32] andC/BE[7..4]#. The master drives PAR64 for address and write data phases; the target drives PAR64 for read data phases.

JTAG/Boundary Pins (Optional)

The IEEE Standard 1149.1 Test Access Port (TAP) and Boundary Scan Architecture is included as an optional interface for PCI devices. The TAP is comprised of four pins (five optional) that are used to interface serially with a TAP controller within the PCI device.

TCK	Test Clock is used to clock state information and test data into and out of the device during operation of the TAP.
TDI	Test Data Input is used to serially shift test data and test instructions into the device during TAP operation.
TDO	Test Output is used to serially shift test data and test instructions out of the device during TAP operation.
TMS	Test Mode Select is used to control the state of the TAP controller in the device.
TRST#	Test Reset provides an asynchronous initialization of the TAP controller. This signal is optional in IEEE Standard 1149.1.

PCI Local Bus Pin Numbering

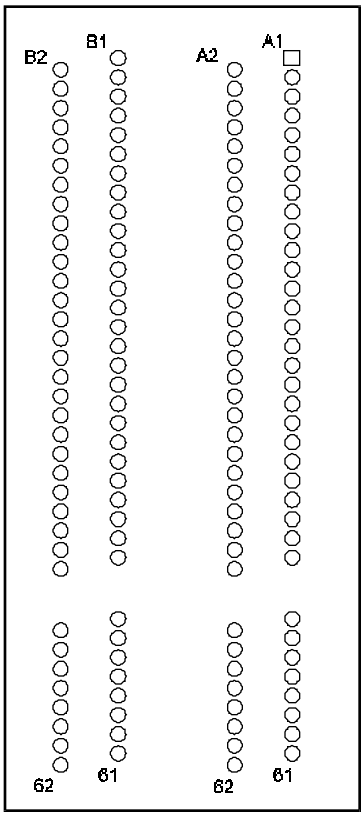

Figure 2-2: 5 Volt 32-bit Connector

PCI Local Bus Pin Assignments

The PCI Local Bus specifies both 5V and 3.3V signaling environments. The bus pin assignments shown in the following tables are for the 5V connector. The 3.3V connector bus pin assignments are the same with the following exceptions:

*	The pins noted as +V (I/O) are +5V or +3.3V, depending on which connector is being used.
†	Pins B12, B13, A12, and A13 are ground on the 5V connector, but are Connector Keys on the 3.3V connector.
††	Pins B50, B51, A50, and A51 are Connectors Keys on the 5V connector, but are ground on the 3.3V connector.

PCI Local Bus Pin Assignments (cont)

I/O Pin	Description	Description	I/O Pin
B1	-12V	TRST#	A1
B2	TCK	+12V	A2
B3	GND	TMS	A3
B4	TDO	TDI	A4
B5	+5V	+5V	A5
B6	+5V	INTA#	A6
B7	INTB#	INTC#	A7
B8	INTD#	+5V	A8
B9	PRSNT1#	RESERVED	A9
B10	RESERVED	+V(I/O)*	A10
B11	PRSNT2#	RESERVED	A11
B12	GND†	GND†	A12
B13	GND†	GND†	A13
B14	RESERVED	RESERVED	A14
B15	GND	RST#	A15
B16	CLK	+V(I/O)*	A16
B17	GND	GNT#	A17
B18	REQ#	GND	A18
B19	+V(I/O)*	RESERVED	A19
B20	AD31	AD30	A20
B21	AD29	+3.3V	A21
B22	GND	AD28	A22
B23	AD27	AD26	A23
B24	AD25	GND	A24
B25	3.3V	AD24	A25
B26	C/BE3#	IDSEL	A26
B27	AD23	+3.3V	A27
B28	GND	AD22	A28
B29	AD21	AD20	A29
B30	AD19	GND	A30
B31	+3.3V	AD18	A31

I/O Pin	Description		Description	I/O Pin
B32	AD17		AD16	A32
B33	C/BE2#		+3.3V	A33
B34	GND		FRAME#	A34
B35	IRDY#		GND	A35
B36	+3.3V		TRDY#	A36
B37	DEVSEL#		GND	A37
B38	GND		STOP#	A38
B39	LOCK#		+3.3V	A39
B40	PERR#		SDONE	A40
B41	+3.3V		SB0#	A41
B42	SERR#		GND	A42
B43	+3.3V		PAR	A43
B44	C/BE1#		AD15	A44
B45	AD14		+3.3V	A45
B46	GND		AD13	A46
B47	AD12		AD11	A47
B48	AD10		GND	A48
B49	GND		AD9	A49
B50	KEY††		KEY††	A50
B51	KEY††		KEY††	A51
B52	AD8		C/BE0#	A52
B53	AD7		+3.3V	A53
B54	+3.3V		AD6	A54
B55	AD5		AD4	A55
B56	AD3		GND	A56
B57	GND		AD2	A57
B58	AD1		AD0	A58
B59	+V(I/O)*		+V(I/O)*	A59
B60	ACK64#		REQ64#	A60
B61	+5V		+5V	A61
B62	+5V		+5V	A62

Table 2-1: 32-bit PCI Connector Pinout

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Chapter 4: Dimensional Drawings

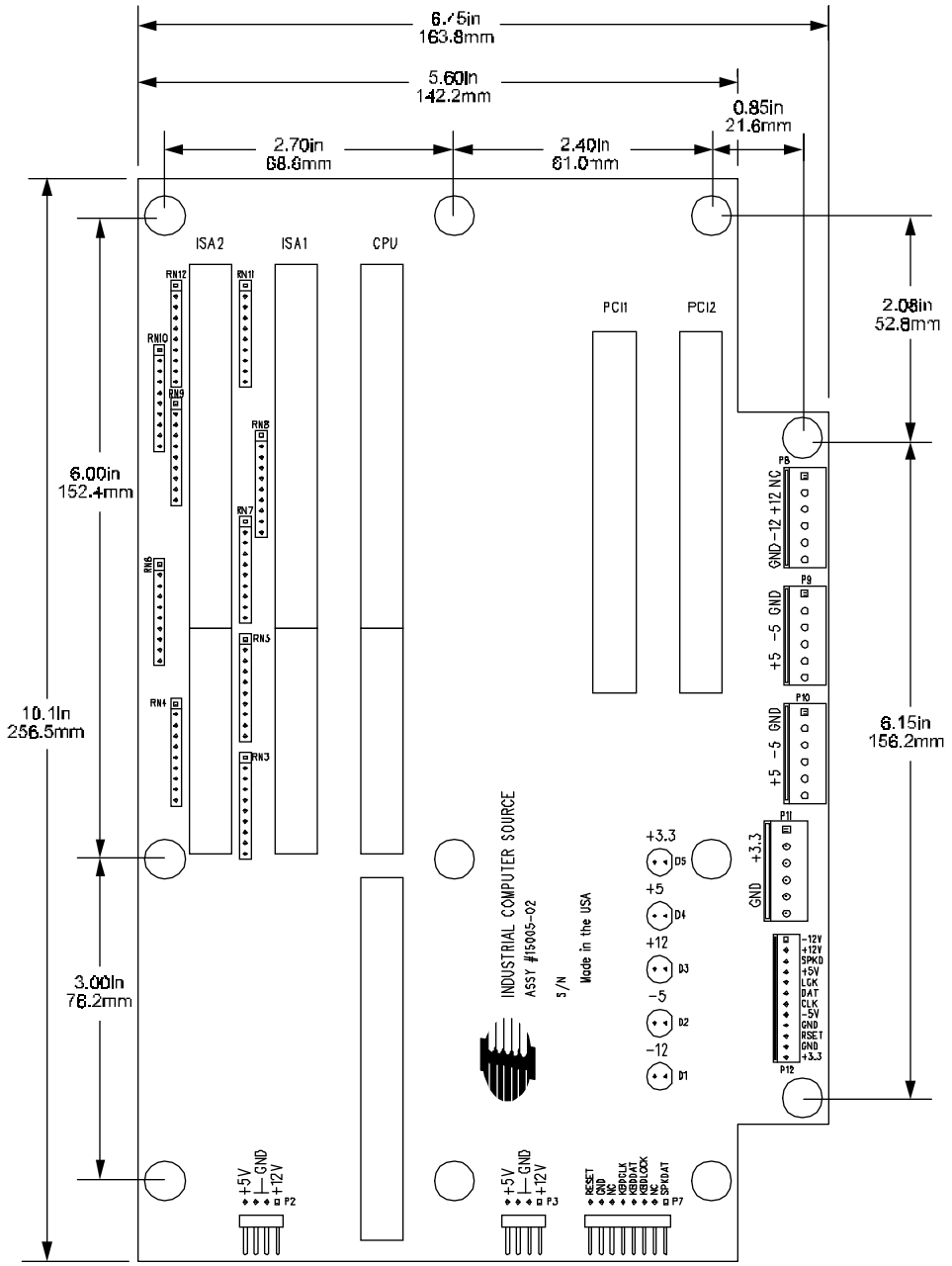

Figure 4-1: 5-slot (15005-02) Backplane

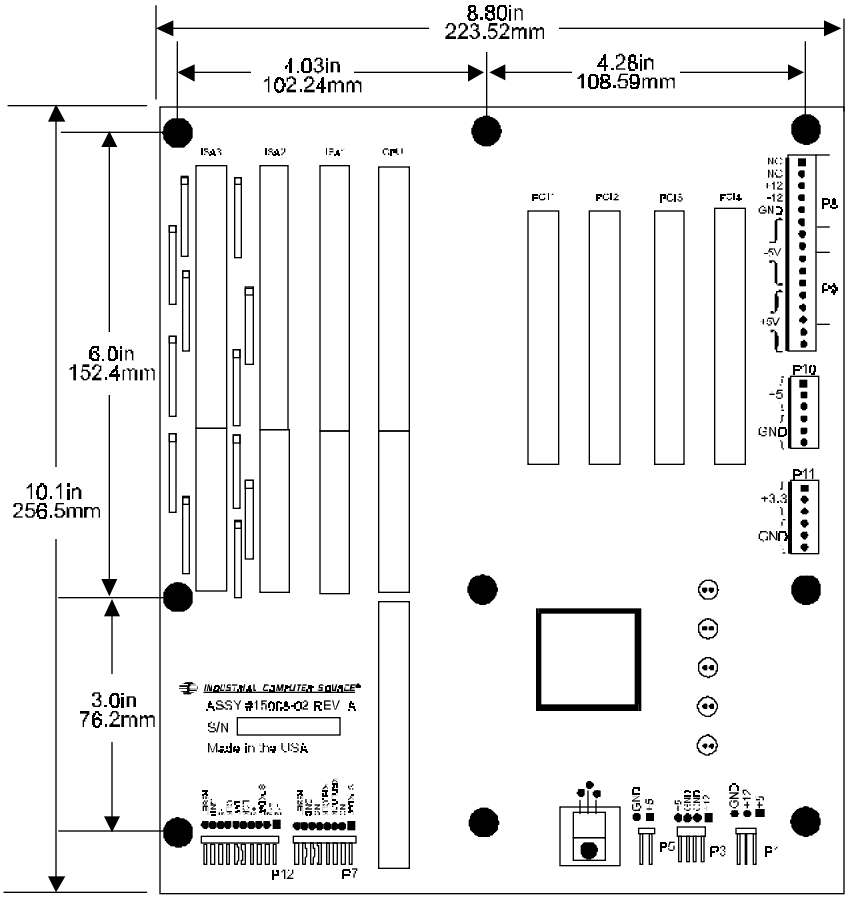

Figure 4-2: 8-slot (15008-02) Backplane

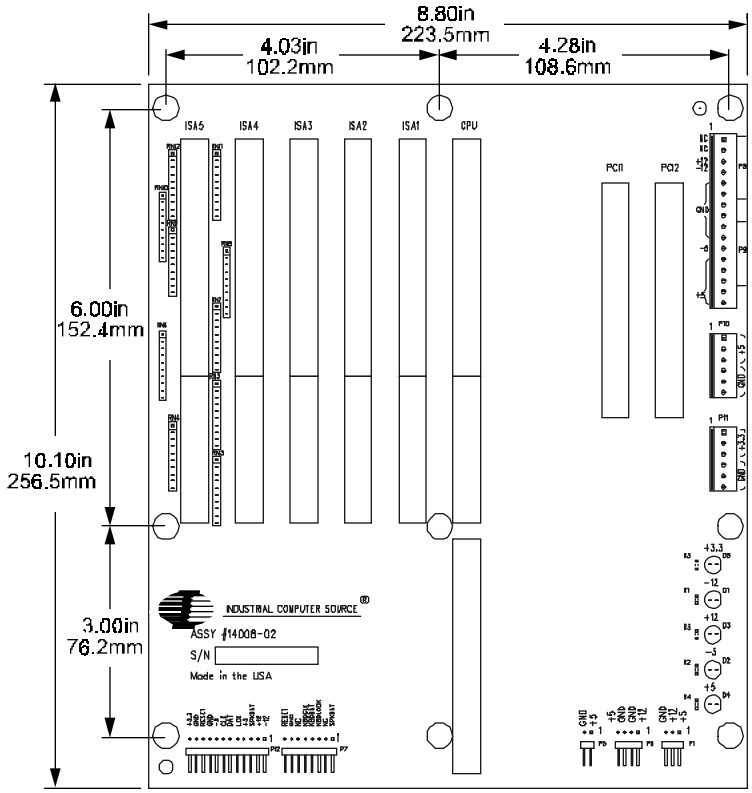

Figure 4-3: 8-slot (14008-02) Backplane

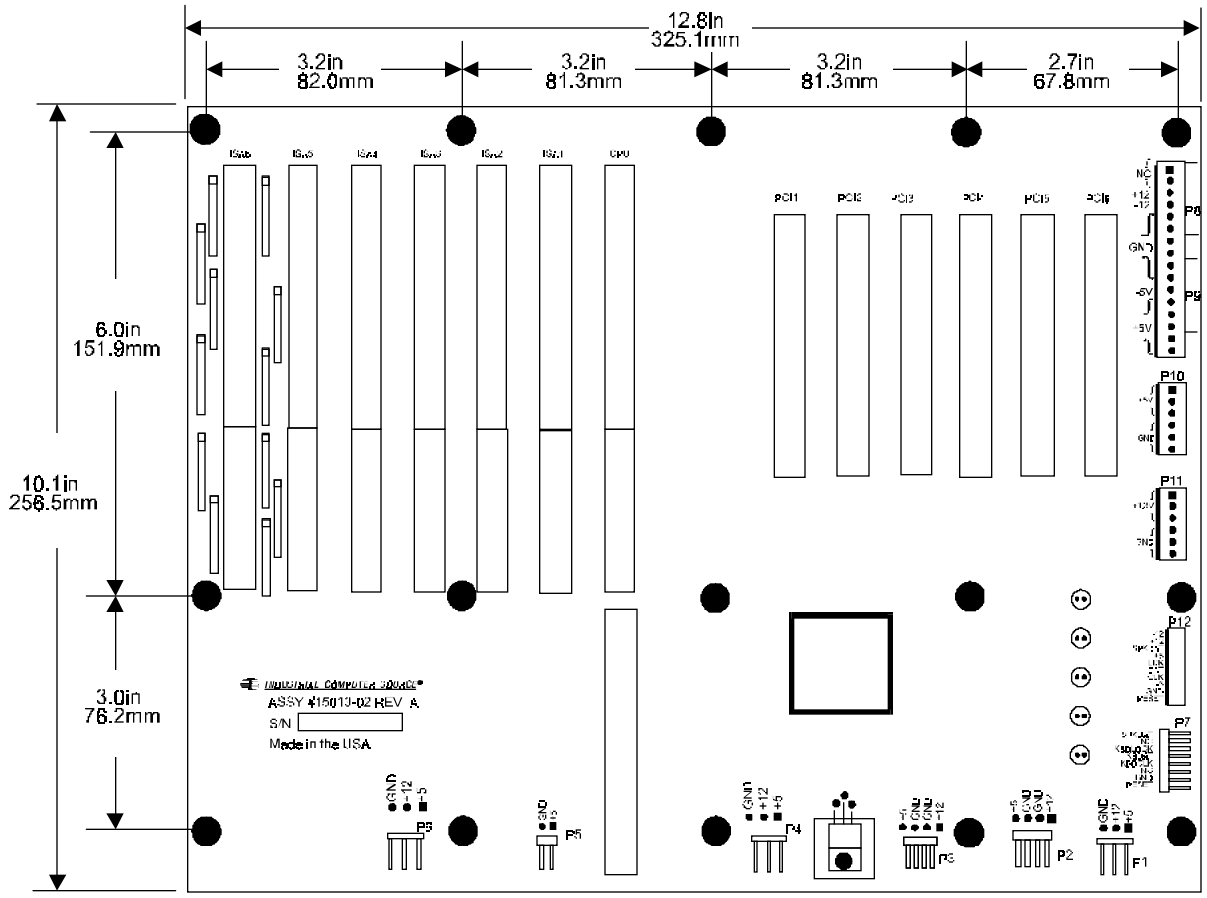

Figure 4-4: 13-slot (15013-02) Backplane

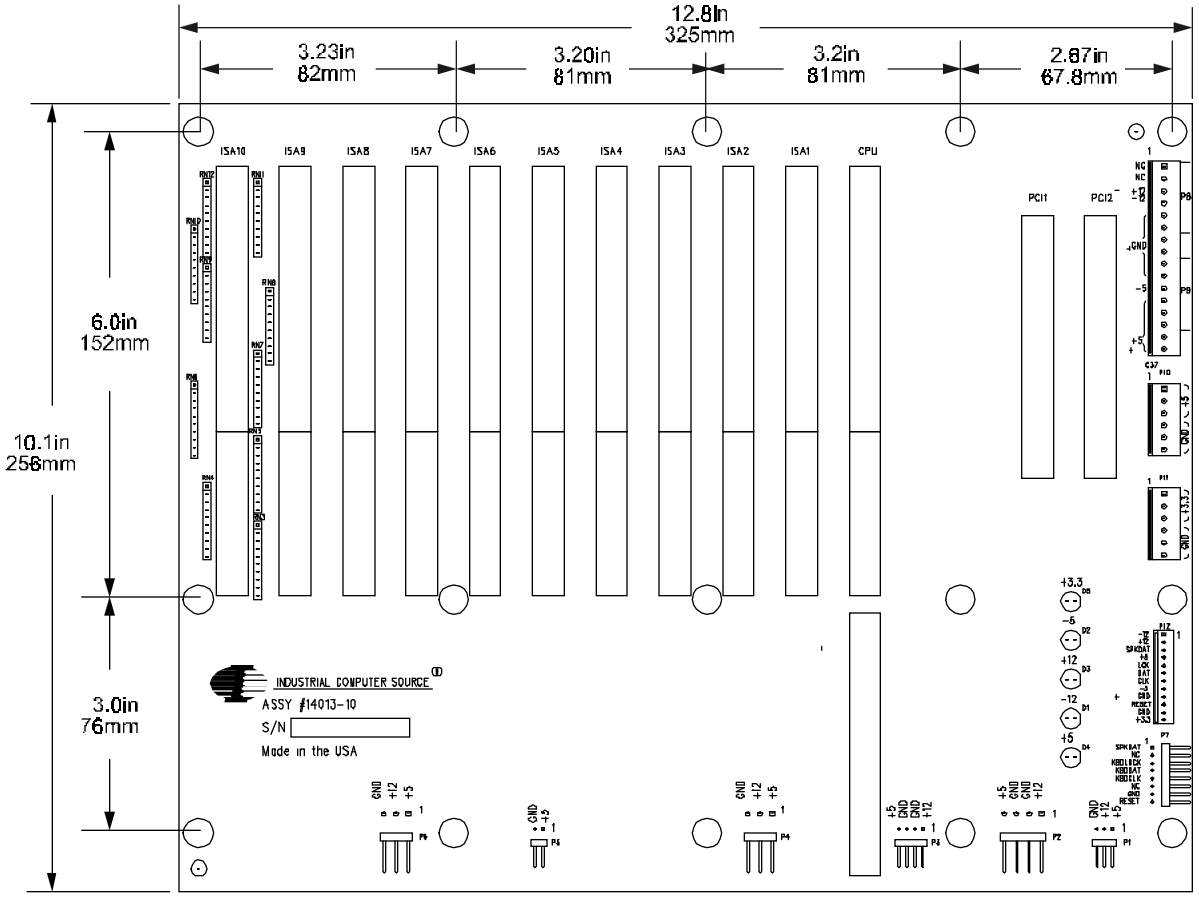

Figure 4-5: 13-slot (14013-10) Backplane

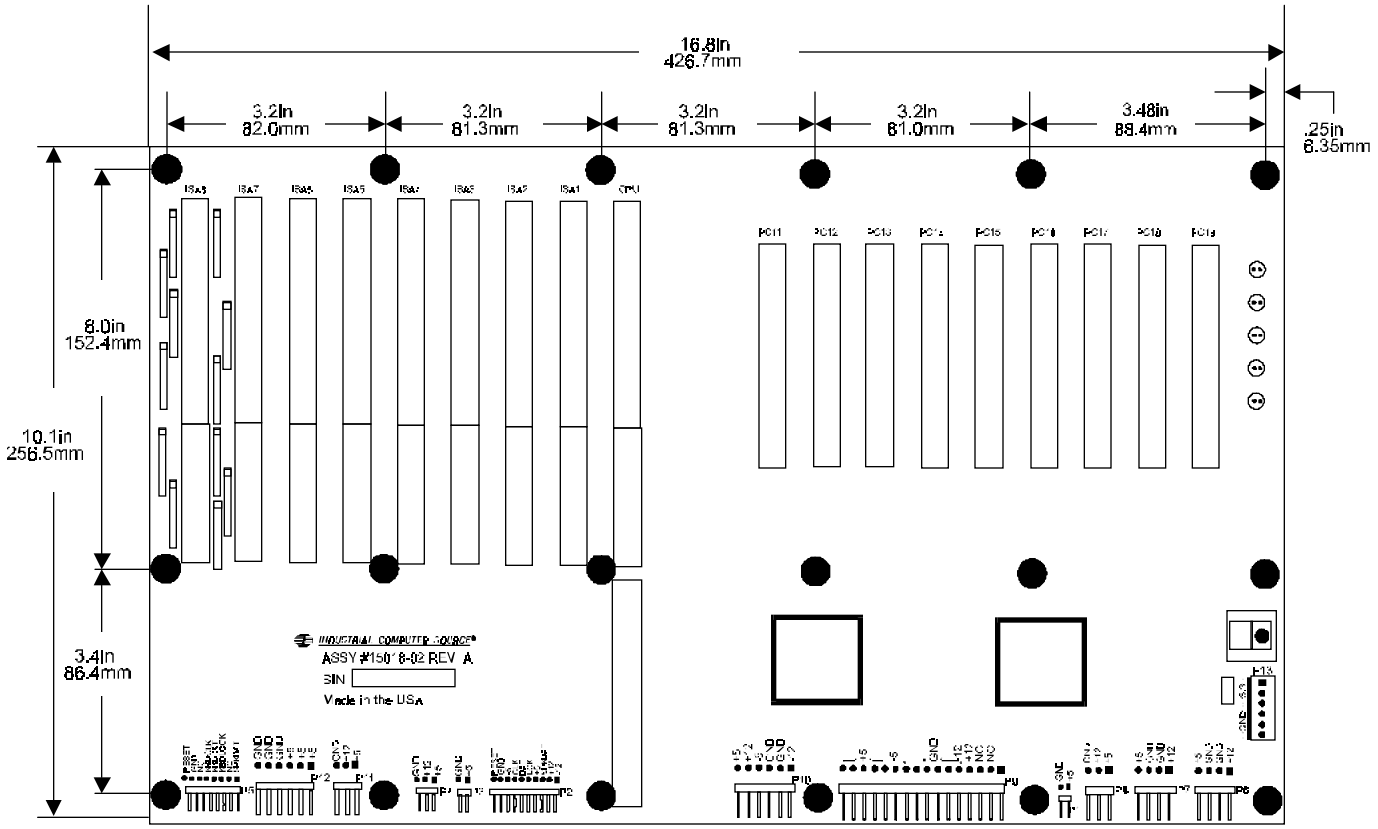

Figure 4-6: 18-slot (15018-02) Backplane

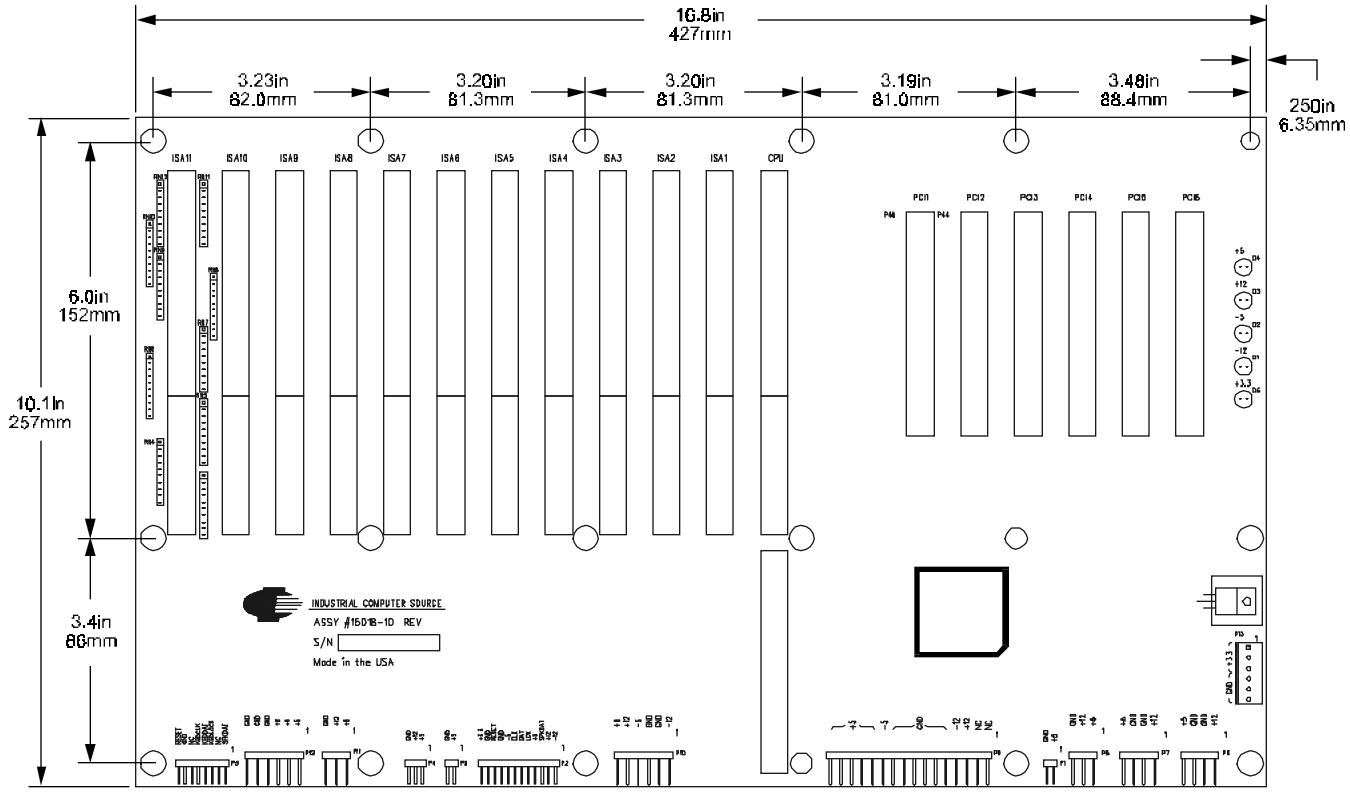

Figure 4-7: 18-slot (15018-10) Backplane

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BUG REPORT

While we have tried to assure this manual is error free, it is a fact of life that works of man have errors. We request you to detail any errors you find on this BUG REPORT and return it to us. We will correct the errors/problems and send you a new manual as soon as available. Please return to:

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