INDUSTRIAL COMPUTER SOURCE®

Model DCC-P
Product Manual

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INDUSTRIAL COMPUTER SOURCE®

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Current Revision 7B

September 1997

Chapter 1: Introduction

The DCC-P series is a family of counter/timer cards consiting of three different models: the DCC5-P, DCC10-P, and the DCC20-P. The DCC20-P contains four AM9513 System Timing Controller LSI circuits. Each AM9513 consits of five independant 16 bit up/down counters. The DCC10-P contains two AM9513 circuits and the DCC5-P contains one. The DCC5-P does however contain an 8 bit input port and an 8 bit output port in addition to the 9513. The DCC10-P and DCC20-P are physically the same board except for the difference in the number of counters. On the DCC10 and DCC20, the signals for each counter are available on independant 26 pin headers; on the DCC5, the signals are available on a DB37 male connector.

Counters

The counters can be programmed to count up or count down in either binary or BCD. A selection of various internal and external frequency sources and outputs may be chosen as inputs for individual counters with software selectable active-high or active-low polarities. Each counter may be gated by either software or hardware.

Each counter has associated with it a Load Register and a Hold Register. Load Registers are used to automatically reload the counter to any predefined value, thus controlling the effective count period.

Hold Registers are used to save count values without disturbing the count process. This permits the processor to read intermediate counts. The Hold Register may also be used as a second Load Register, in some modes. Counters 1 and 2 have additional alarm registers and comparators associated with them plus logic for operations in a 24-hour time-of-day mode. The time-of-day logic will accept 50Hz, 60Hz, and 100Hz input frequencies.

Each counter has a single dedicated output pin. Considerable versatility for configuring both the input and the gating of individual counters is provided. This not only permits dynamic re-assignment of inputs under software control, but also allows multiple counters to use a single input, allows a single gate input to control more than one counter, and allows for cascading.

Crystal Timebase

An 8Mhz crystal oscillator is provided on the card. It provides a 1Mhz clock input for the counters.

Digital I/O

The DCC5-P also contains an 8-bit, latched, parallel digital, TTL input port and an 8 bit, latched, parallel digital, TTL output port. The output port features tri-state outputs designed specifically for driving capacitive or low-impedance loads. Outputs can source up to 24mA and can drive 15 standard TTL loads or 60 low-power Schottky TTL loads.

Interrupts

Interrupts from counter outputs or external sources are supported. An output from a PAL is connected to any one of interrupt levels IRQ2 through IRQ7 which are user-selected by jumper installation on the card. The DCC10 and DCC20 also support IRQ9 through IRQ12, IRQ 14, and IRQ 15. On the DCC-P, if an Interrupt Enable input at I/O connector pin 2 is held high, the interrupt function is disabled. Conversely, if the Interrupt Enable input is held low, a rising edge on the Interrupt Input, pin 1, will generate an interrupt on the selected level. It is the user's responsibility to set up and enable the 8259 controller in the computer, the interrupt vectors, and an interrupt service routine.

Typically, counter outputs can be jumpered to the Interrupt Input and the Interrupt Enable can be controlled by one of the digital output bits. This allows software control of a periodic interrupt, for example.

Software

The files contained on the provided diskette may be copied onto your hard disk. Files contained on the disk are stored in separate directories. Refer to the README.TXT file on the diskette for more information about these files.

Specifications

Sample Modes for the 9513 Timer

Software-Triggered Strobe w/No Hardware Gating
Software-Triggered Strobe w/Level Gating
Hardware-Triggered Strobe

Rate Generator w/Synchronization (Event Counter with Auto-Read/Reset)
Rate Generator w/No Hardware Gating
Rate Generator w/Level Gating

Retriggerable One-Shot
Non-Retriggerable One-Shot

Hardware-Triggered Delayed-Pulse One-Shot
Hardware-Triggered Delayed Pulse Strobe

Software-Triggered Delayed-Pulse One-Shot
Software-Triggered Delayed-Pulse One-Shot w/ Hardware Gating

Variable Duty Cycle Rate Generator w/No Hardware Gating
Variable Duty Cycle Rate Generator w/Level Gating

Software-Triggered Strobe w/Level Gating and Hardware Retriggering
Software-Triggered Strobe w/Edge gating and Hardware Retriggering

Frequency Shift Keying

Inputs

Voltage: One LSTTL load

Logic High:	2.0 to 5.0 VDC
Logic Low:	-0.5 to 0.8 VDC

Hysteresis (Source & Gate):	0.2V min., 0.3V typical
Switching Characteristics:	See Appendix A
Maximum Input Frequency:	7 MHz

Outputs

Counter Outputs: Can sink 3.2 mA and source 200 uA

F_{out}: Can sink 3.2 mA and source 200 uA.

Digital Output Port (DCC5-P Only): Can drive up to 15 standard TTL loads or 60 low-power Schottky loads.

Enviromental

Operating Temperature Range:	0^{0} to 50^{o} C.
Storage Temperature Range:	-25^{o} to $+85^{o}$ C.
Humidity:	0 to 90% RH, non-condensing
Power Required:	+5 VDC at 400 mA typical

Agency Approvals

CE Conformity with:

EU EMC Directive 89/336/EEC

EU Low Voltage Directive 72/23/EEC

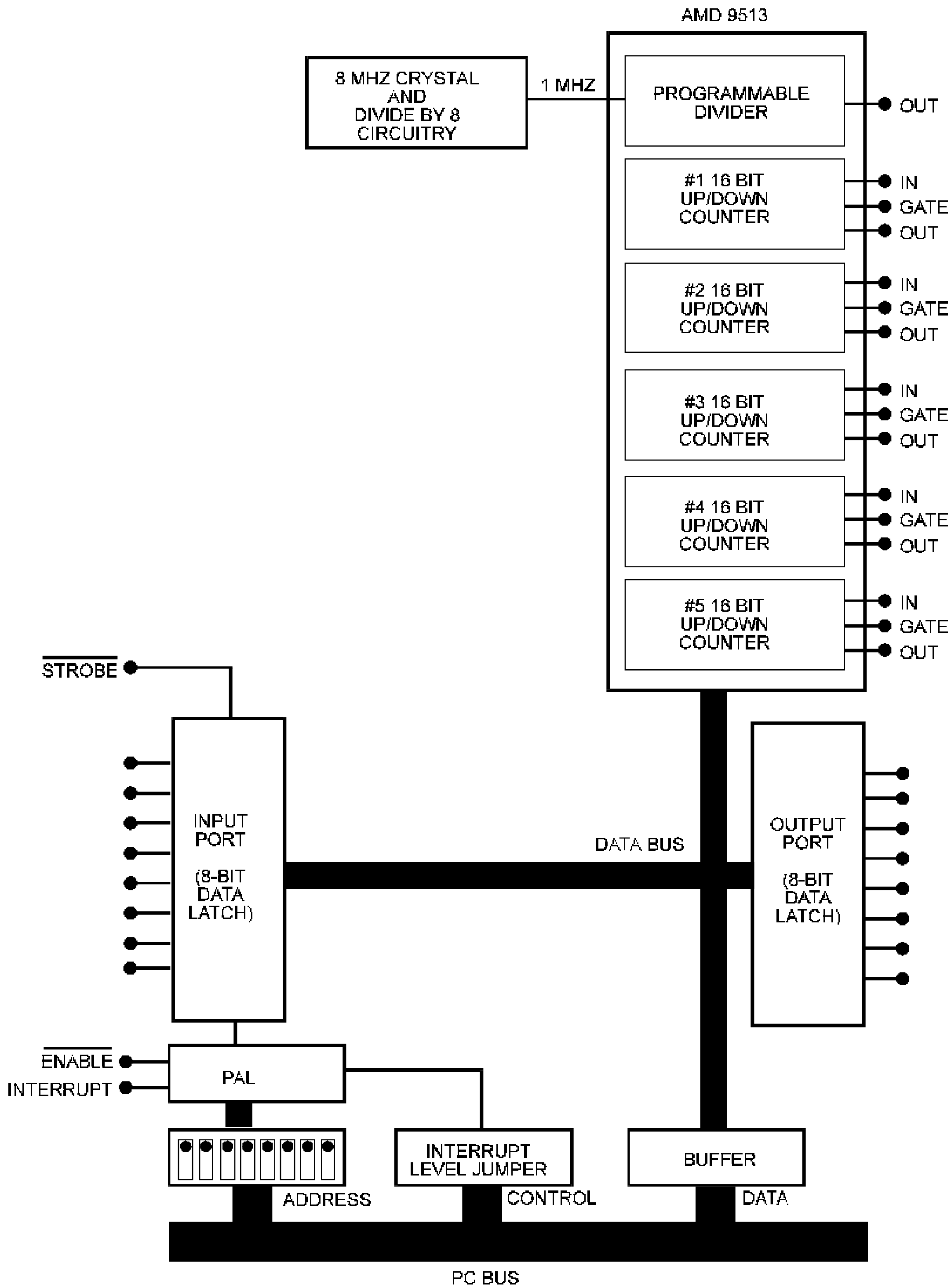

Figure 1-1: DCC5 Block Diagram

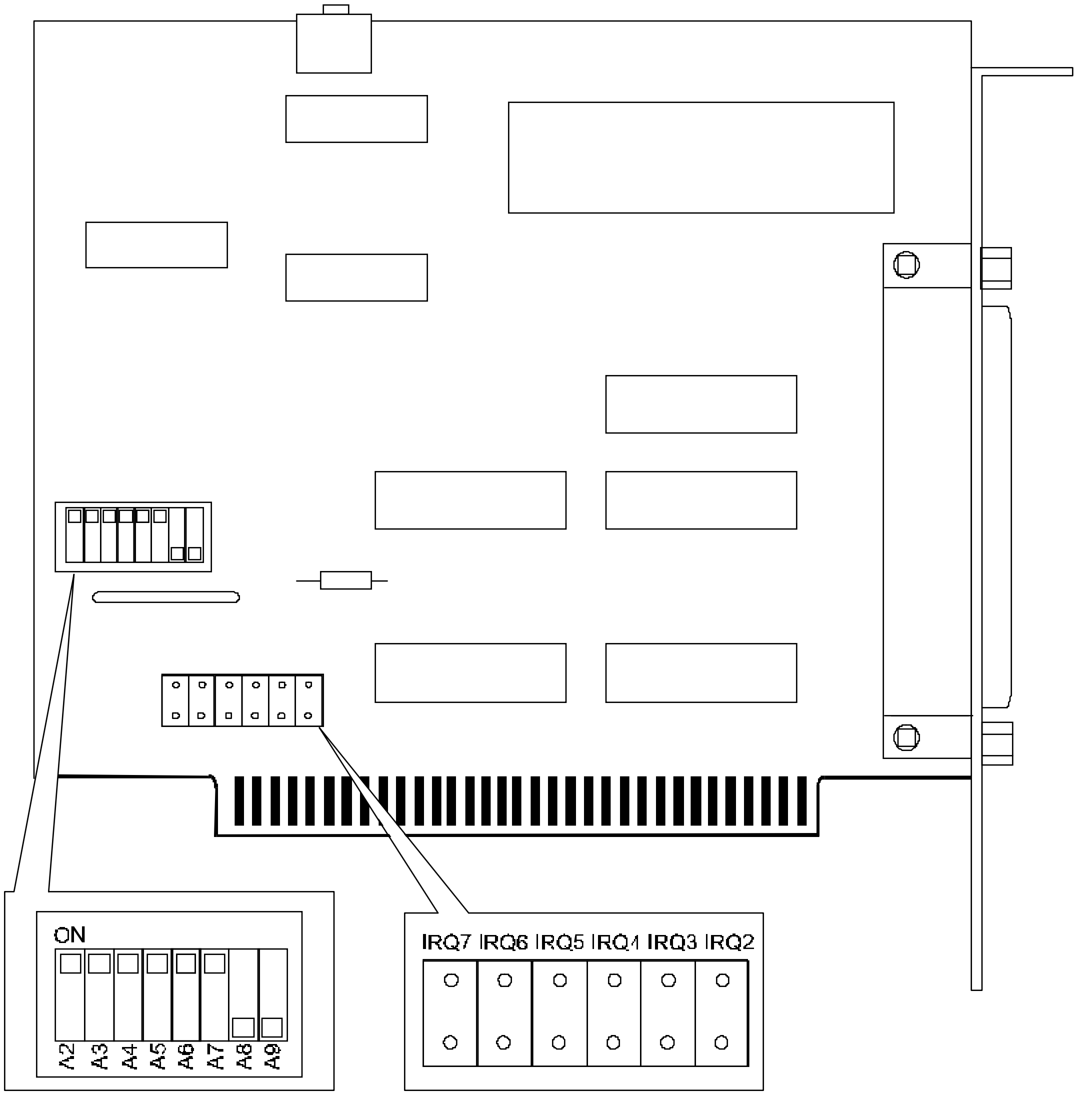

Figure 1-2: DCC5 Board Layout

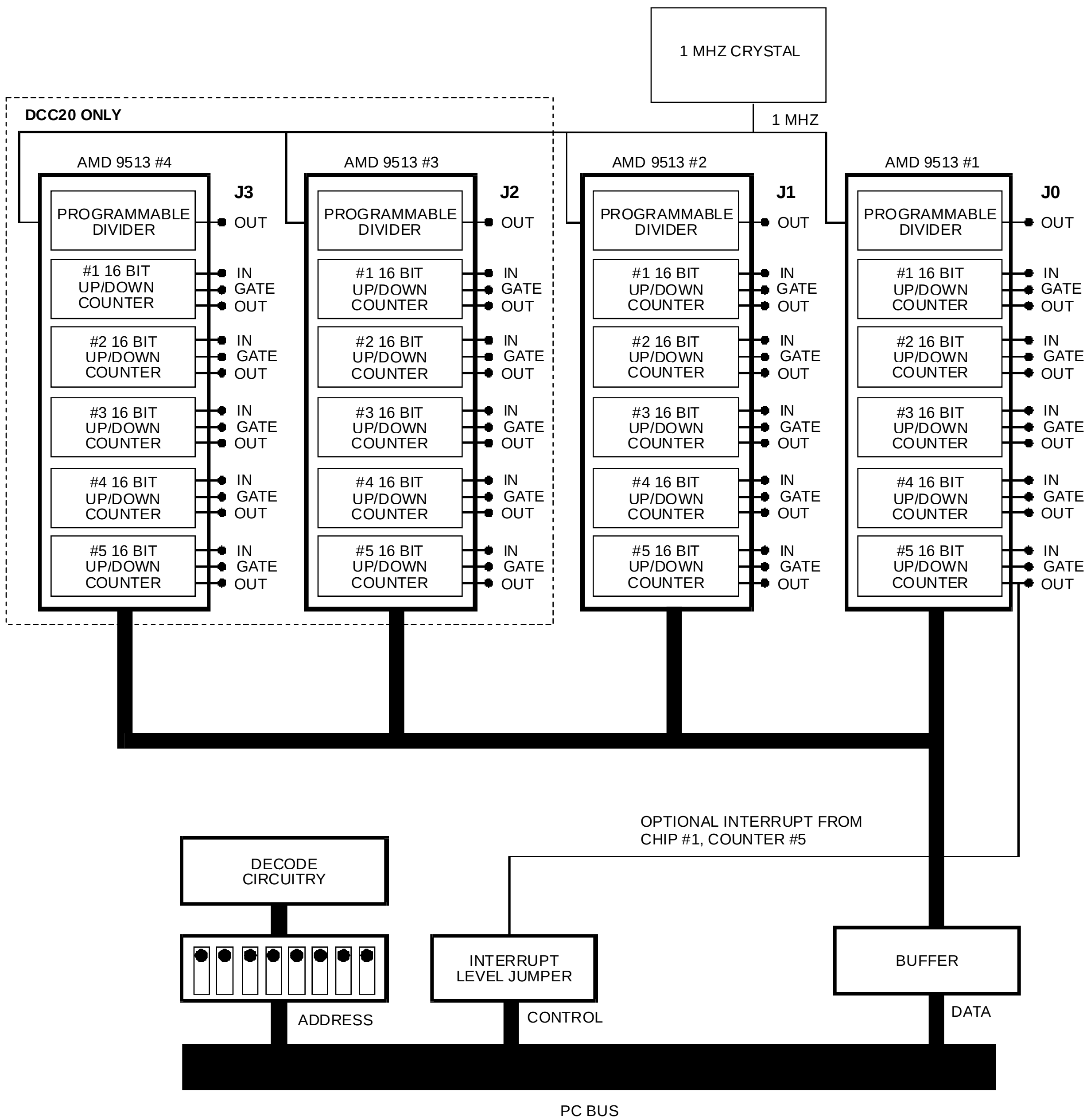

Figure 1-3: DCC10/DCC20 Block Diagram

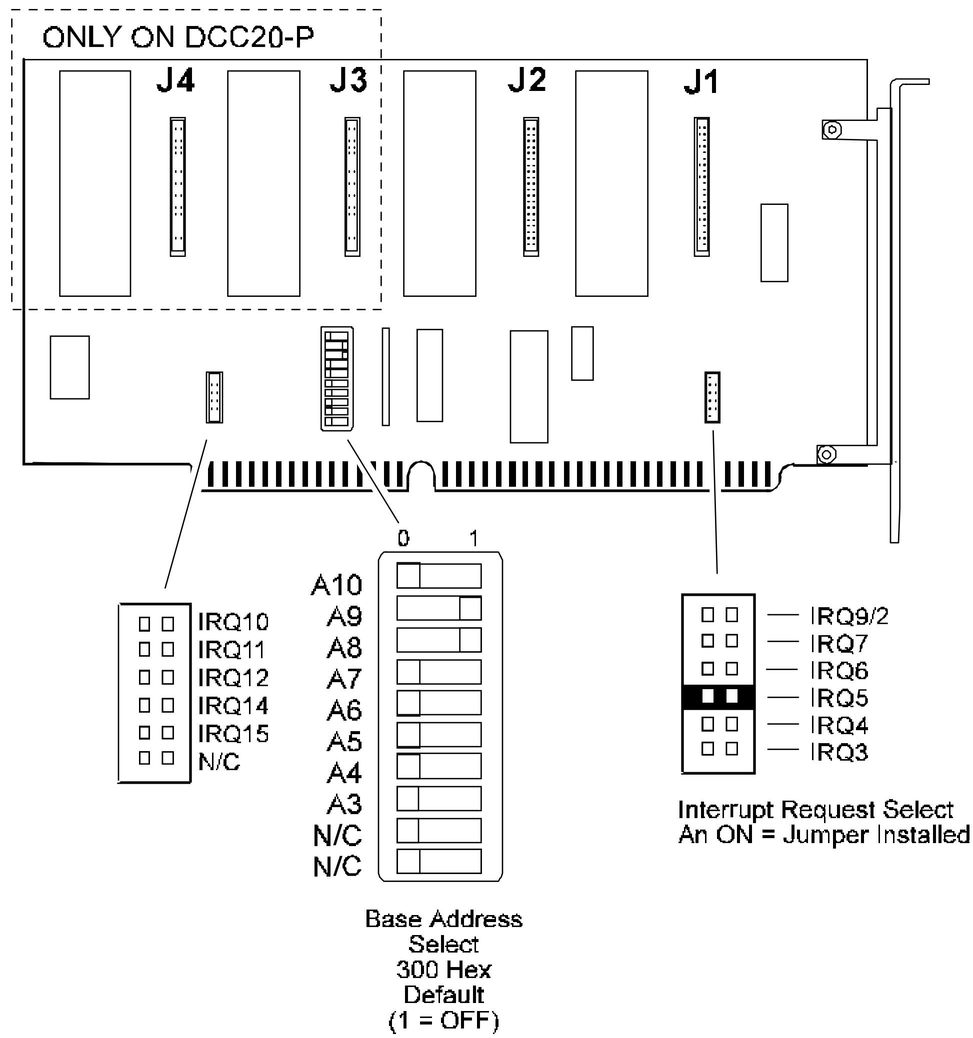

Figure 1-4: DCC10/DCC20 Board Layout

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Chapter 2: Installation

Installation Overview

To perform a complete installation, complete the following:

1. Perform the Installation Precheck Procedure.
2. Set the base address of the card.
3. Set the IRQ jumper.
4. Install the board.

Address Selection

The DCC5, DCC10, and DCC20 use four, six, and eight consecutive addresses in I/O address space, respectively. The base or starting address can be selected anywhere within the I/O address range 100H-3FFH for the DCC5 and 100H-7FFH on the DCC10 or DCC20, provided it does not cause an overlap with other functions. If in doubt about what base address to use, the following table lists standard address assignments. Addresses not mentioned in this table are generally available for I/O boards.

Hex Range	Usage
000-0FF	Internal System - Not Usable
1F0-1FF	AT Hard Disk
200-207	Game Control
278-27F	Parallel Port (LPT2)
238-23B	Bus Mouse
2E8-2EF	Asynchronous Communications (COM4)
2F8-2FF	Asynchronous Communications (COM2)
300-31F	Prototype Card
320-32F	XT Hard Disk
378-37F	Parallel Port (LPT1)
380-38F	SDLC Communications
3A0-3AF	SDLC Communications
3B0-3BB	MDA
3BC-3BF	Alt. Parrallel Port
3C0-3CF	EGA
3DO-3DF	CGA
3E8-3EF	Asynchronous Communications (COM3)
3F0-3F7	Floppy Disk
3F8-3FF	Asynchronous Communications (COM1)

The board's base address is set up by a DIP switch. The switch controls address bits A3 through A9 for the DCC5 and A3 through A10 for the DCC10 and DCC20. (Lines A2 and A0 are used on the card to control individual registers. Descriptions of these lines are in the Programming chapter of this manual.)

To determine how to set these switches for a desired hex-code address, refer to the Address Settings table. If you prefer to determine proper switch settings yourself, first convert the hex-code address to binary form (refer to the Address Values and Switch Settings table). Then, set the corresponding switch to ON for each “0” and set the corresponding switch to OFF for each “1”.

The following example illustrates switch selection corresponding to hex 300(or binary 11 0000 0xxx). The “xxx” represents address lines A2-A0 which are used on the card to select individual registers as described in the Programming section of this manual.

Address Settings

	A10	A9	A8	A7	A6	A5	A4	A3
200H	ON	OFF	ON	ON	ON	ON	ON	ON
210H	ON	OFF	ON	ON	ON	ON	OFF	ON
220H	ON	OFF	ON	ON	ON	OFF	ON	ON
300H	ON	OFF	OFF	ON	ON	ON	ON	ON
310H	ON	OFF	OFF	ON	ON	ON	OFF	ON
320H	ON	OFF	OFF	ON	ON	OFF	ON	ON
350H	ON	OFF	OFF	ON	OFF	ON	OFF	ON
700H	OFF	OFF	OFF	ON	ON	ON	ON	ON

Address Values and Switch Settings

Address Line	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Binary	0	0	1	1	0	0	0	0	0	0	0	0
Hex	3				0				0			
Switch Settings			OFF	OFF	ON	ON	ON	ON	ON			

ON=0 OFF=1

Carefully review the address selection reference table before selecting the card address and then perform the Installation Precheck Procedure to determine if that address is in fact free. If the addresses of two installed items overlap, you will experience unpredictable computer behavior.

A10 has been added to the DCC10 and DCC20 to literally double its available I/O address space. However, due to the inability off other boards to interpret A10, address overlap may occur without the actual addresses overlapping. An example of this would be if another board uses address 300h and the DCC10/20 is set to use 700h. Now, we send a read command to 700h to obtain information from the DCC10/20. If the board using 300h can not interpret A10, it will also respond because the only difference between 300h and 700h is A10. To avoid this problem, simply set A10 to "ON" and do not use the additional address space.

Installation Precheck Procedure

The precheck procedure is designed to help you determine if the address you have selected for the board is actually free for use. In the following example we are testing for an address of hex 300, but any other address may be substituted.

1. Type DEBUG at the DOS prompt and the press the Enter key. The DOS directory must be in your path statement or you must change to the DOS subdirectory before running this application. The DEBUG "-" prompt is displayed.

2. Type i 300 at the DEBUG "-" prompt and press the Enter key. This reads I/O address H300. DEBUG returns an FF if the address is not currently in use. If a value other than FF is returned, the address is being used by another board. Try each desired address until an FF is returned.

For information about the various functions available through DEBUG, simply type a ? at the prompt and press the Enter key.

3. Repeat step 2 for the next seven addresses, since the board uses up to eight consecutive addresses. For example, if 300 checked out, check 301, 302, and 303. Each of these addresses should also return an FF.

4. Type q and press the Enter key to exit DEBUG.

5. After you have finished checking each address, type q and press the Enter key to exit DEBUG.

6. Turn off the computer in preparation for installing the circuit board. If you haven't already done so, set the address switches in accordance with the directions in the previous section.

Installing the Board

CAUTION!

Be sure to turn off the power to the computer before installing the board. Failure to do so could cause damage to the board or computer, invalidating the warranty

To install the board, perform the following steps:

1. Turn off the computer and remove the cover of the case.
2. Select an empty, standard size slot and remove the screw at the top of the slot's backplate.
3. Remove the backplate.
4. Plug the board into the empty slot. Ensure that the board is firmly seated in the slot.
5. Reinstall the screw removed in step 2. Ensure that the board is securely fastened in place.
6. Reinstall the cover of the case.

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Chapter 3: Programming

I/O Addresses

The DCC5, DCC10, and DCC20 use four, six, and eight consecutive addresses in I/O address space, respectively. Available addresses are from hex 200 to hex 3FC. The base or starting address is selected by a DIP switch as described in the Address Selection section of this manual and automatically falls on a 4-bit boundary. The address maps for the appropriate boards are as follows:

DCC5-P		
I/O Address	**Write**	**Read**
Base + 0	9513 Data Write	9513 Data Read
Base + 1	9513 Command	9513 Status
Base + 2	invalid	Digital Input IP0-7
Base + 3	Digital Output OP0-7	invalid

DCC10/20			
Chip	**I/O Address**	**Write**	**Read**
1	Base+0	9513 Data Write	9513 Data Read
	Base+1	9513 Command	9513 Status
2	Base+2	9513 Data Write	9513 Data Read
	Base+3	9513 Command	9513 Status
DCC20 Only			
3	Base+4	9513 Data Write	9513 Data Read
	Base+5	9513 Command	9513 Status
4	Base+6	9513 Data Write	9513 Data Read
	Base+7	9513 Command	9513 Status

Byte-Oriented Operation

If you are using an AT class computer, note that all ports are eight bits wide (one byte) and you should perform byte-oriented read/write operations rather than word (16 bits) operations. When performing consecutive byte transfers to the same I/O port on an AT, be sure to allow sufficient recovery time for the I/O circuits.

9513 Register Functions

All data transfers to the 9513 LSI counter timer chip are performed through two I/O ports. Since there are a number of internal registers in the 9513 LSI chip, an indirect system of accessing those registers is used via an internal data pointer register which, in turn, is reached through the command register. The Data port (Base +0) is used for data transfer; i.e., loading and reading registers. The Command port (Base +1) is used for addressing registers. The Command port also performs other functions such as loading and enabling the counters, latching counter contents, etc. (Appendix A of this manual contains a data sheet with detailed information on the 9513 LSI chip.)

Indirect Addressing

The basic premise behind indirect addressing is to first point to the register you wish to access. To do this, you use the data pointer register which is one of several specific uses for the Command port (Base +1). Then you load or read the data via 2 writes or reads to the Data port (Base +0). Because of this, most functions require at least three lines of code. To simplify programming slightly, the 9513 also uses the Command port (Base +1) to perform other frequently used commands with a single write. This is explained further in the following programming section.

Programming Sequence

Setup and initialization of this board follows a very basic procedure. The necessary steps and code examples that follow outline this procedure. The various registers and bit definitions on the following pages can be modified for use in your own application.

Doing a Master Reset to the board, before the initialization sequence, is a good idea. Write "FF" to the Command Register of each chip before initializing the board.{1st chip base+1, 2nd chip base+3}. It is not always necessary to do a Master Reset but some operating systems require it.

In the following steps, delays have not been added. Whenever two OUT statements follow one another in a compiled language, a delay must be added between them to allow for hardware recovery time. To insert a delay, simply use an empty loop as follows:

```
For X= 1 to 2: Next X
```

Initialization Sequence

1. Set the Master Mode (MM) register. This initializes the board. Refer to the Master Mode Register section later in this chapter for bit definitions for this register.

```
OUT BASEADDR+1, &H17          'Write to Data Pointer Register to point to the
                              'Master Mode Register.
OUT BASEADDR, &HB0            'Load LSB of MM register.
OUT BASEADDR, &H40            'Load MSB of MM register.
```

This particular example sets the board in the following configuration:

-Binary scalar division
-Data Pointer Increment disabled
-8 bit bus (always)
-Fout active
-Fout = Fout source/16
-Compare & Time-of-Day disabled

2. Set Counter Mode (CM) register for each counter. Refer to the Counter Mode Register section later in this chapter for bit definitions for this register.

```
OUT BASEADDR+1, &H01          'Point to the Counter 1 Mode Register (CM1).
OUT BASEADDR, &H22            'Load LSB of CM1 register.
OUT BASEADDR, &H01            'Load MSB of CM1 register.
OUT BASEADDR+1, &H02          'Point to Counter Mode Register (CM2).
OUT BASEADDR, &H00            'Load LSB of CM2 register.
OUT BASEADDR, &H22            'Load MSB of CM2 register.
```

This sets the counters (1 and 2) to the following modes:

Counter 1:

-No gating (special gate disabled)
-Count on rising edge
-Counter source from SRC1 pin
-Reload from load register
-Count repetitively
-Count binary
-Count down
-Toggle output on terminal count

Counter 2:

-No gating

-Count on rising edge

-Counter source is output of Counter 1

-Reload from load register

-Count repetitively

-Count in binary

-Count down

-Toggle output on terminal count

3. Fill each Counter Load Register with a starting value (which is automatically reloaded into the counter after each terminal count.)

```
OUT BASEADDR+1, &H09          'Point to the Counter 1 Load Register.
OUT BASEADDR, &HFF            'Load LSB of C1 Load Register.
OUT BASEADDR, &HFF            'Load MSB of C1 Load Register.
OUT BASEADDR, &H0A            'Point to Counter 2 Load Register.
OUT BASEADDR, &H00            'Load LSB of C2 Load Register.
OUT BASEADDR, &H80            'Load MSB of C2 Load Register.
```

4. Load counters (transfer contents of load register into counter). See the Command description section later in this chapter for more information on using this command.

```
OUT BASEADDR+1, &H43          'Loads Counter 1 and 2.
```

5. Arm counters (this begins the count cycle.)

```
OUT BASEADDR+1, &H21          'Arms counter 1.
OUT BASEADDR+1, &H22          'Arms counter 2.
```

Note: To arm both counters simultaneously, use OUT BASEADDR+1, &H23.

Saving, Reading, and Disarming the Counters

1. Save the count (put the current count into the Counter Hold Register while counting continues undisturbed):

```
OUT BASEADDR+1, &HA3          'Saves counter 1 and 2.
```

2. Read the count from the Counter Hold Register:

```
OUT BASEADDR+1, &H11          'Point to Counter 1 Hold Register.
CTR1LO=INP(BASEADDR)          'Read the LSB.
CTR1HI=INP(BASEADDR)          'Read the MSB.
OUT BASEADDR+1, &H12          'Point to Counter 2 Hold Register.
CTR2LO=INP(BASEADDR)          'Read the LSB.
CTR2HI=INP(BASEADDR)          'Read the MSB.
```

3. Disarm counters when done.

```
OUT BASEADDR+1, &HC1          'Disarms counter 1.
OUT BASEADDR+1, &HC2          'Disarms counter 2.
```

Master Mode Register

The 16-bit Master Mode (MM) register controls the overall operation of the board and should be initialized by your program. It is a 16-bit register and, in the following description, bit locations are listed as MM15 through MM0 which correspond to the most significant bit through the least significant bit.

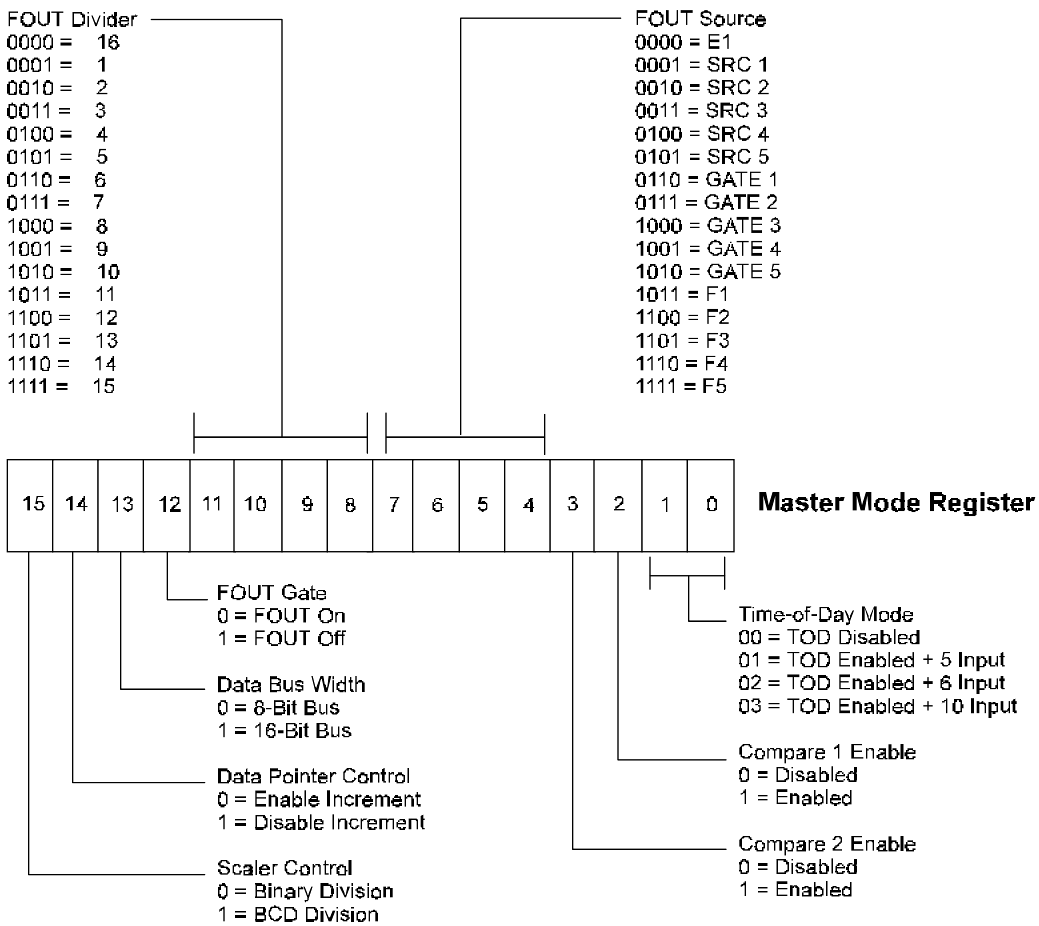


Figure 3-1: Master Mode Register Bit Assignments

Master Mode Register Bit Assignments

Function	Properties
Scaler Ratios	Master Mode bit MM15 controls the counting configuration of the Frequency Scaler counter. When MM15 = 0, the Scaler divides the oscillator frequency in binary steps so that each subfrequency is 1/16 of the preceding frequency. When MM15 = 1, the Scaler divides in BCD steps so that adjacent frequencies are related by ratios of 10 instead of 16.

Data Pointer Sequencing	Bit MM14 controls the Data Pointer Logic to enable or disable the automatic sequencing functions. When MM14 = 1, the contents of the Data Pointer can be changed only directly by entering a command. When MM14 = 0, several types of automatic sequencing of the Data Pointer are available. These are described in the Data Pointer register section of the data sheet at the back of this manual.
Bus Width	Bit MM13 controls the multiplexer at the data bus interface in order to configure the part for an 8-bit or 16-bit external bus. The DCC-P Series uses an 8-bit bus.
FOUT Gate	Master Mode bit MM12 provides a software gating capability for the FOUT signal. When MM12 = 1, FOUT is off and in a low-impedance state to the ground.
FOUT Divider	Bits MM8 through MM1 specify the dividing ratio for the FOUT Divider. The FOUT source (selected bye bits MM4 through MM7) is divided by an integer value between 1 and 16, inclusive, and is then passed to the FOUT output buffer.
FOUT Source	Master Mode bits MM4 through MM7 specify the source input for the FOUT divider. Fifteen inputs are available for selection and they include the five Source pins, the five Gate pins and the five internal frequencies derived from the oscillator and the scaler.
Comparator Enable	Bits MM2 and MM3 control the Comparator associated with the Controllers 1 and 2. When a Comparator is enabled, its output is substituted for the normal counter output on the associated OUT1 or OUT2 pin. See the data sheet at the back of this manual for more information.
Time-of-Day	Bits MM0 and MM1 of the Master Mode register specify the Time-of-Day (TOD) options. When MM0 = 0 and MM1 = 0, the special logic used to implement the TOD is disabled and Counter 1 and 2 will operate in exactly the same way as Counter 3, 4, and 5. When MM0 =1 or MM1 = 1, additional counter decoding and control logic is enabled on Counters 1 and 2, which causes their decades to turn over at the counts that generate appropriate 24-hour TOD accumulations. For additional information, see the Time-of-Day chapter in the 9513A System timing controller technical manual.

Counter Mode Register

The Counter Mode register for each counter should be initialized after the Master Mode register. The Counter Mode registers are 16-bit registers and the bit locations are designated CM15 through CM0, which correspond to the most significant bit to the least significant bit. Each Counter uses a separate Counter Mode (CM) register allowing the individual counters to operate independently. These options include output configuration, count control, count source and gating control. The following figure shows the bit assignments for the Counter Mode registers. This section describes the control options in detail. Note that generally each counter is independently configured and does not depend on modes of other counters. The Counter Mode register should be loaded only when the counter is Disarmed. Attempts to load the Counter Mode register when the counter is armed may result in erratic counter operation.

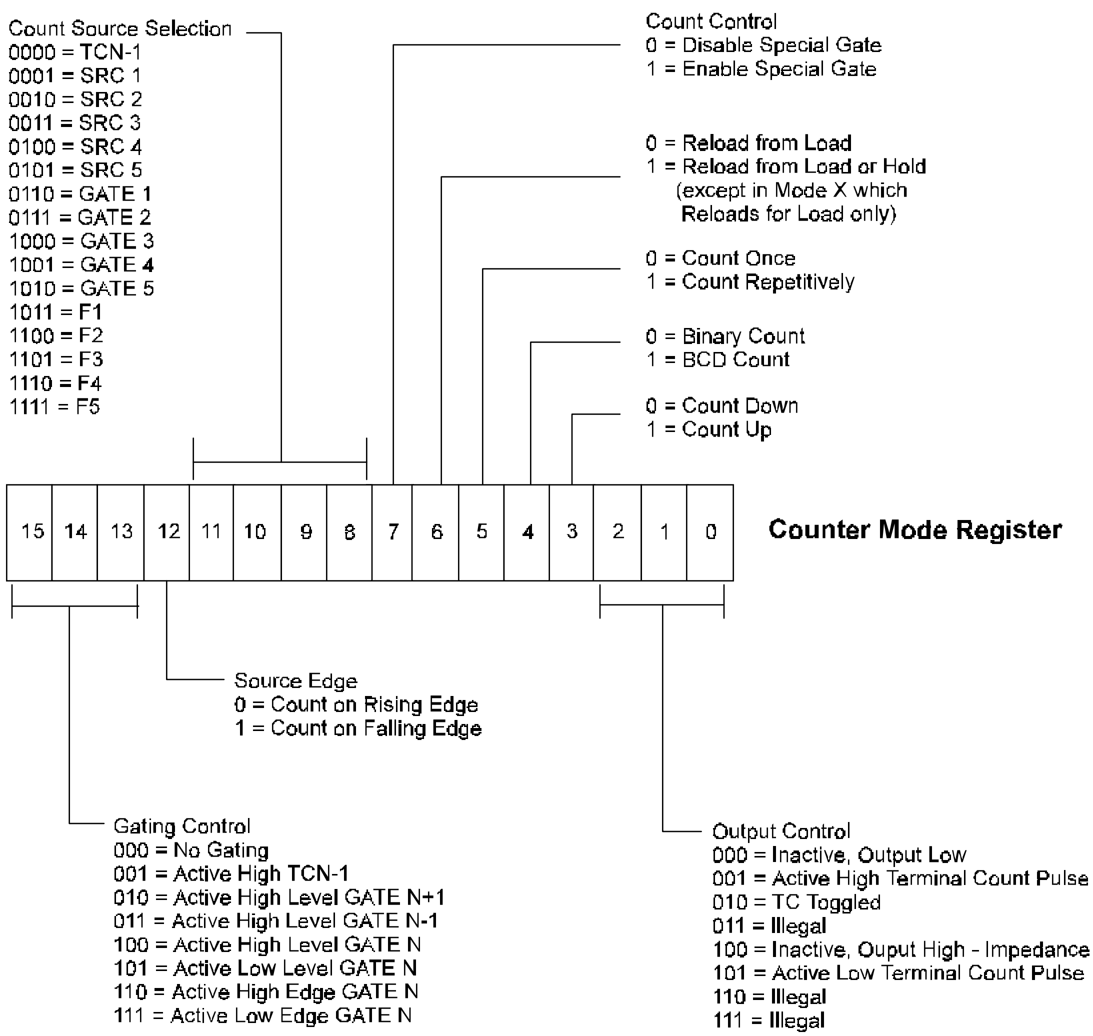


Figure 3-2: Counter Mode Register Bit Assignments

Counter Mode Register Bit Assignments

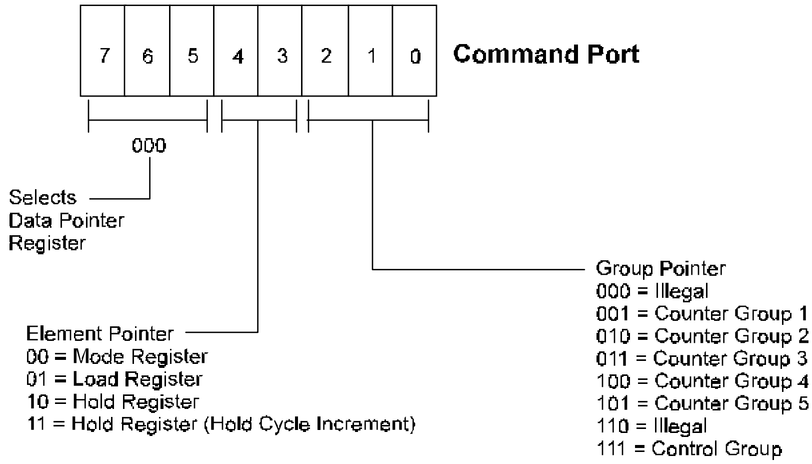
Function	**Properties**
Gating Control:	Counter Mode bits CM15, CM14, and CM13 specify the hardware gating options. When "no gating" is selected (000), the counter will proceed unconditionally as long as it is armed. For any other gating mode, the count process is conditioned by the specified gating configuration.
Counter Source Selection:	Counter Mode bits CM8 through CM12 specify the source used as input to the counter and the active edge that is counted. Bit CM12 controls the polarity for all the sources; logic zero counts rising edges and logic one counts falling edges. Bits CM8 through CM11 select 1 of 16 counting sources to route to the counter input. Five of the available inputs are internal frequencies derived from the internal oscillator. Ten of the available inputs are interface pins; five are labeled SRC and five are labeled GATE. The 16th available input is the TC output from the adjacent lower-numbered counter. (The Counter 5 TC wraps around to the Counter 1 input.)
Count Control:	Counter Mode bits CM3 through CM7 specify the various options available for direct control of the counting process. CM3 and CM4 operate independently of the others and control up/down and BCD/binary counting. Bit CM5 controls the repetitions of the count process. When CM5 = 1, counting will proceed in the specified mode until the counter is disarmed. When CM5 = 0, the count process will proceed only until one full cycle of operation occurs. This may occur after one or two TC events. Bit CM7 controls the special gating functions that allow retriggering and the selection of Load or Hold sources for counter reloading.
Output Control:	Counter mode bits CM0 through CM2 specify the output control configuration. The OUT pin may be off (a high impedance state), or it may be inactive with a low-impedance to ground. The three remaining valid combinations represent the active-high, active-low, or TC toggle output waveforms.

Data Pointer Register

The Data Pointer Register is set using the information in the following figure. For detailed information about the Data Pointer Register, refer to the data sheet at the back of this manual. As discussed in the Programming Sequence Section of this chapter, this register points to other registers in the 9513. It navigates through the various registers of the 9513's indirect addressing scheme. The Data Pointer Register is selected with a write to Base +1 where the three most significant bits must be 000.

Command Port (Base +1)

The Command port of the 9513 has many different functions, including loading, arming, and saving the counters. It also allows access to the counter registers via the Data Pointer Register. The various functions are indicated by the three most significant bits.



Command Descriptions (BASE+1)

Six of the command types are used for direct software control of the counting process and they each contain a 5-bit S field. In a linear-select fashion, each bit in the S field corresponds to one of five general counters (S1=Counter 1, S2=Counter2, etc.). When an S bit is a one, the specified operation is performed on the counter so designated; when an S bit is a zero, no operation occurs for the corresponding counter.

Arm Counters

C7	C6	C5	C4	C3	C2	C1	C0
0	0	1	S5	S4	S3	S2	S1

Any combination of counters, as specified by the S field, will be enabled for counting. A counter must be armed before counting can commence. Once armed, the counting process may be further enabled or disabled using the hardware gating facilities.

Load Counters

C7	C6	C5	C4	C3	C2	C1	C0
0	1	0	S5	S4	S3	S2	S1

Any combination of counters, as specified in the S field, will be loaded with previously entered values. The source of information for each counter will be either the Load register or the Hold register, as determined by the operating configuration in the Mode register.

Load and Arm Counters

C7	C6	C5	C4	C3	C2	C1	C0
0	1	1	S5	S4	S3	S2	S1

Any combination of counters, as specified in the S field, will be first loaded then armed. This command is equivalent to issuing a LOAD command and then ARM command.

Disarm Counters

C7	C6	C5	C4	C3	C2	C1	C0
1	1	0	S5	S4	S3	S2	S1

Any combination of counters, as specified by the S field, will be disabled from counting. A disarmed counter will cease all counting independent of other conditions.

Save Counters

C7	C6	C5	C4	C3	C2	C1	C0
1	0	1	S5	S4	S3	S2	S1

Any combination of counters, as specified by the S field, will have their contents transferred into their associated Hold register. The transfer takes place without interfering with any counting that may be underway. This command will overwrite any previous Hold register contents.

Disarm and Save Counters

C7	C6	C5	C4	C3	C2	C1	C0
1	0	0	S5	S4	S3	S2	S1

Any combination of counters, as specified by the S field, will be disarmed and the contents of the Counter register will be transferred into the associated Hold registers.

Master Reset

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	1	1	1	1	1

The Master Reset command duplicates the action of the power-on reset circuitry. It disarms all counters, enters Hex 0000 in the Master Mode, Load and Hold registers and enter 0B00 hex in each of the Counter Mode Registers. Doing a Master Reset to the board, before the initialization sequence, is a good idea. Write "FF" to the Command Register of each chip before initializing the board. {1st chip base+1, 2nd chip base+3}. It is not always necessary to do a Master Reset but some operating systems require it.

Peek and Poke Driver for Windows 95/NT

This driver allows developers to write Win32 programs which access hardware I/O ports and physical memory. This should allow easier testing of hardware components since they can be accessed without the use of a specific driver.

It should be noted that this driver will give application level access to areas of the hardware and memory which can quite easily crash the operating system or even corrupt data. Care needs to be taken to only access known memory or I/O ports.

Using The Library

There are two libraries that can be used to ease use of the Peek and Poke driver. They are pplib95.lib and pplibnt.lib. They are used for Windows 95 and Windows NT respectively. These libraries provide I/O routines familiar to those who have used Microsoft compilers in the past.

To use a library, add pplib95.lib or pplibnt.lib to your link, whichever is appropriate for the target OS. Include pplib95.h or pplibnt.h in the C/C++ file you will be accessing the functions from. These libraries are compatible with all Microsoft compilers. NOTE: These libraries are not thread safe.

The following is a list of the functions provided by the library.

Function	Description
BOOL ics_pp_open (void)	Opens the Peek and Poke driver. Returns TRUE if successful. This must be called before any calls are made to the other library functions.
void ics_pp_close (void)	Closes the driver. Should be called before the application exits.
void *ics_pp_make_pointer (int page, int length)	This function is used to allow access to a particular region of physical memory by a Win32 application. page is the starting page of the physical memory. length is the size of the region in pages. For example, for a pointer to a region of physical memory starting at 0xA0000 and 64k long: void *ptr = ics_pp_make_pointer (0xA0, 0x10); The pointer can then be treated as a standard C/C++ pointer. NOTE: Be sure to release this memory region back to the system with a call to ics_pp_release_pointer. (See Below.)
void ics_pp_release_pointer (void *address, int length)	This function is used to release a memory mapping made with ics_pp_make_pointer. It is important to release such pointers back to the system. Failure to do so could affect the way the system runs even after the application has exited. address is the address that was returned by the ics_pp_make_pointer function. length is the size of the mapped region in pages.
int _outp (USHORT port, int data) USHORT _outpw (USHORT port, USHORT data) ULONG _outpl (USHORT port, ULONG data)	These functions output data to the given port. Use _outp for byte width, _outpw for word width, and _outpl for double word width.
Int _inp (USHORT port) USHORT _inpw (USHORT port) ULONG _inpl (USHORT port)	These functions return data input from the given port. Use _inp for byte width, _inpw for word width, and _inpl for double word width.

PeekPoke Driver for Windows NT Installation

This driver allows developers to write WinNT programs which access hardware I/O ports and physical memory.

Installing the Windows NT PeekPoke Driver

Under Windows NT 3.51:

- From the Program Manager, click on File->Run.
- Type a:\setup and press OK.

From Windows NT 4.0

- From the Start Menu, select Run.
- Type a:\setup and press OK.

The InstallShield installer will initialize and run. Follow the on-screen instructions. You will need to provide one piece of information:

- The destination path for the driver files.

When the files are transferred, you will be asked if you want to reboot the computer. The drivers will not work until after a reboot.

PeekPoke Driver for Windows 95 Installation

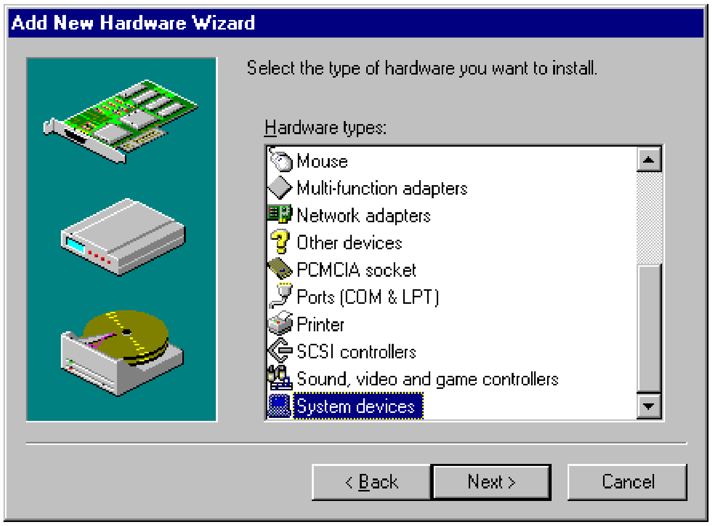
This driver allows developers to write Win95 programs which access hardware I/O ports and physical memory.

Installing the Windows 95 PeekPoke Driver

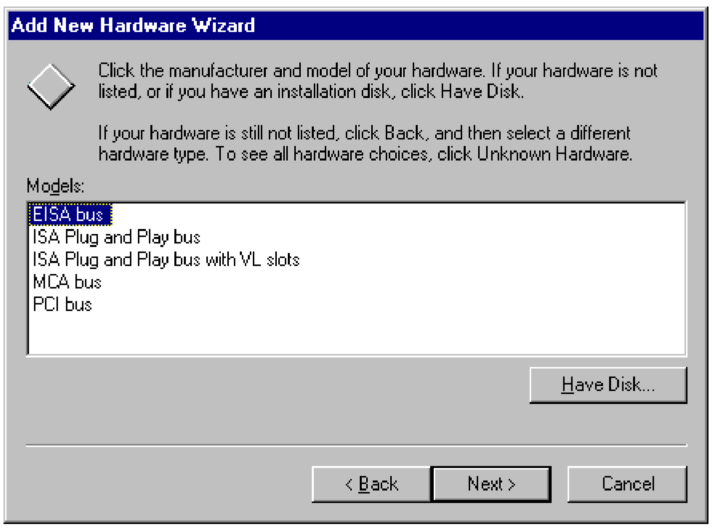
- From the Start Menu, select Settings->Control Panel.
- From the Control Panel, select Add New Hardware.

- Click the Next button.

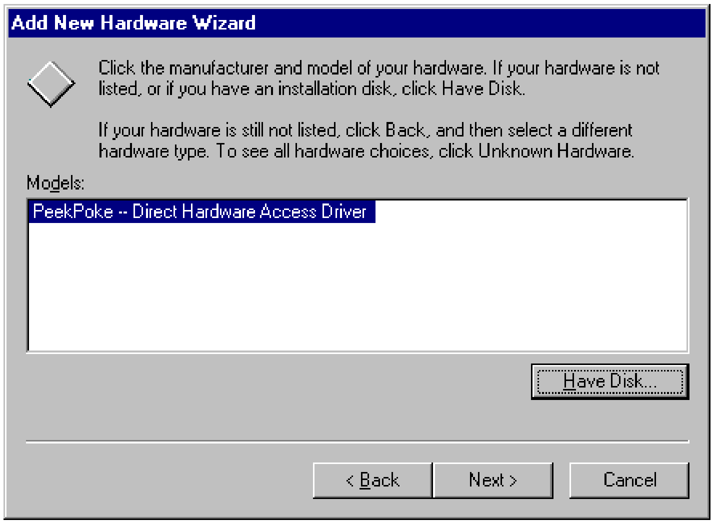
- Answer “No” to the question, “Do you want Windows to search for you new hardware?”
- Press the Next button.



- Scroll the hardware types list down and select the "System devices" type.
- Press the Next button.



- Press the Have Disk button.
- Insert your disk labeled "Windows 95 PeekPoke Driver Disk."
- Make sure "A:\" is selected as the source.
- Press OK.



- The model “PeekPoke – Direct Hardware Access Driver” should be selected in the Models box.
- Press the Next button.
- Windows 95 will copy the driver’s files onto your system.
- Press the Finish button.
- At this point, you will need to shutdown and reboot your machine for the changes to take effect.

Chapter 4: Calibration

A trimmer capacitor on the DCC5-P card can change the crystal oscillator frequency by ±0.01%. If you are not using the internal frequency source in your application or if 0.1% accuracy is satisfactory for your application, then there is no need to adjust this frequency. The DCC10 and DCC20 do not provide this adjustment.

The internal crystal source can be readily adjusted to 0.001% but remember that it has a temperature coefficient of 1 PPM/^{o}C and an aging characteristic of under 3 PPM/year.

To calibrate the crystal, connect an accurate frequency counter to F_{out} (pin 30) and digital common (pin 11). An extender card will be helpful in providing access to the DCC5-P card. After the computer is rebooted, the DCC5-P is reset, the output frequency will default to 62.500 KHz (1 MHz/16). Adjust the trimmer capacitor for a reading of 62.5000 KHz using a 10-second gate interval on the frequency counter.

That’s a rather long gate interval so, if you prefer you can use a 1 second gate interval with an F_{out} of 1 MHz using the following procedure. Enter DEBUG and type the following three commands (assuming a base address of H300):

```
- o 301, 17
- o 300, 00
- o 300, 01
```

After the third line, the frequency will change to 1 MHz and the adjustment can be performed to 1.000000 MHz.

How to remain CE Compliant

In order for machines to remain CE compliant, only CE compliant parts may be used. To keep a chassis compliant it must contain only compliant cards, and for cards to remain compliant they must be used in compliant chassis. Any modifications made to the equipment may affect the CE compliance standards and should not be done unless approved in writing by Industrial Computer Source.

The DCC-P Family is designed to be CE Compliant when used in an CE compliant chassis. Maintaining CE Compliance also requires proper cabling and termination techniques. The user is advised to follow proper cabling techniques from sensor to interface to ensure a complete CE Compliant system. Industrial Computer Source does not offer engineering services for designing cabling or termination systems. Although Industrial Computer Source offers accessory cables and termination panels, it is the user's responsibility to ensure they are installed with proper shielding to maintain CE compliance.

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Chapter 5: Connector Pin Assignments

Counter and digital I/O signals are connected to the DCC5-P card via a 37-pin D type connector that extends through the back of the computer case. The mating connector is an AMP 747304-1 or equivalent. Pin assignments are as follows:

Pin	Name	Function
1		Interrupt Input
2		(not) Interrrupt Enable
3	OP7	Digital Output Bit 7
4	OP6	Digital Output Bit 6
5	OP5	Digital Output Bit 5
6	OP4	Digital Output Bit 4
7	OP3	Digital Output Bit 3
8	OP2	Digital Output Bit 2
9	OP1	Digital Output Bit 1
10	OP0	Digital Output Bit 0
11	GND	Digital Common
12	GATE5	Counter 5 Gate
13	SRC5	Counter 5 Input
14	GATE4	Counter 4 Gate
15	SRC4	Counter 4 Input
16	GATE3	Counter 3 Gate
17	SRC3	Counter 3 Input
18	GATE2	Counter 2 Gate
19	SRC2	Counter 2 Input

Pin	Name	Function
19	SRC2	Counter 2 Input
20	+5VDC	+5 Volt Power (from computer)
21		(not) IP Strobe
22	IP7	Digital Input 7
23	IP6	Digital Input 6
24	IP5	Digital Input 5
25	IP4	Digital Input 4
26	IP3	Digital Input 3
27	IP2	Digital Input 2
28	IP1	Digital Input 1
29	IP0	Digital Input 0
30	FOUT	Oscillator Out
31	OUT5	Counter 5 Output
32	OUT4	Counter 4 Output
33	OUT3	Counter 3 Output
34	OUT2	Counter 2 Output
35	OUT1	Counter 1 Output
36	SRC1	Counter 1 Input
37	GATE1	Counter 1 Gate

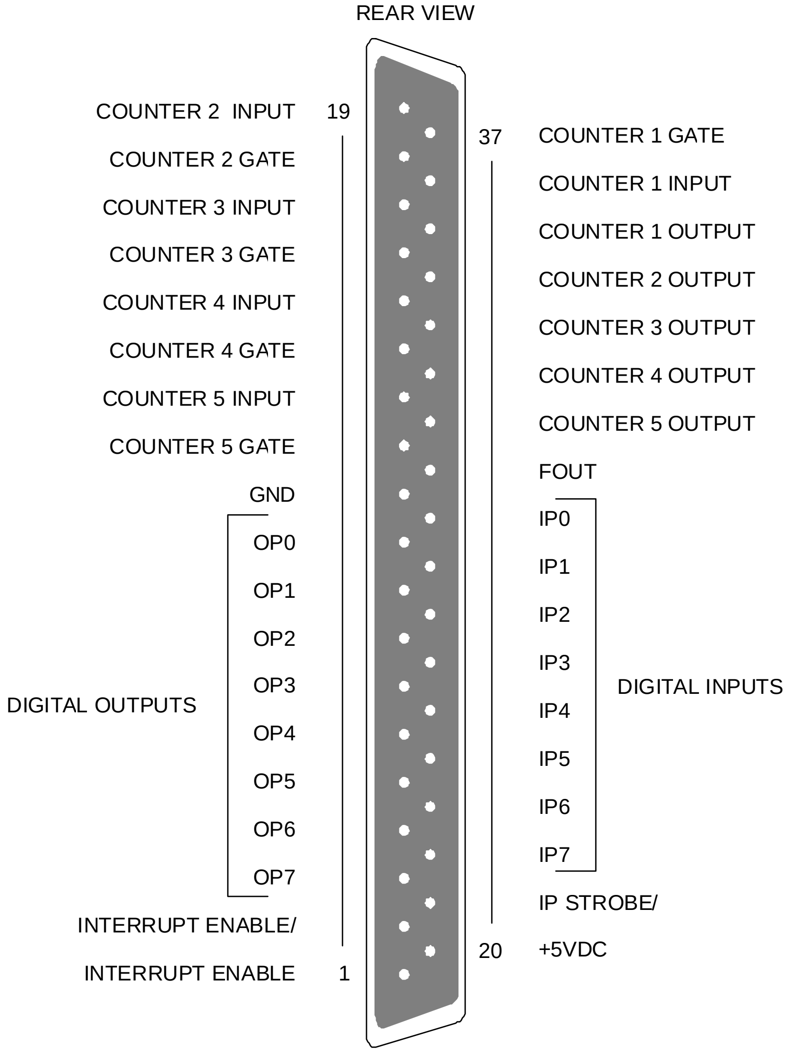
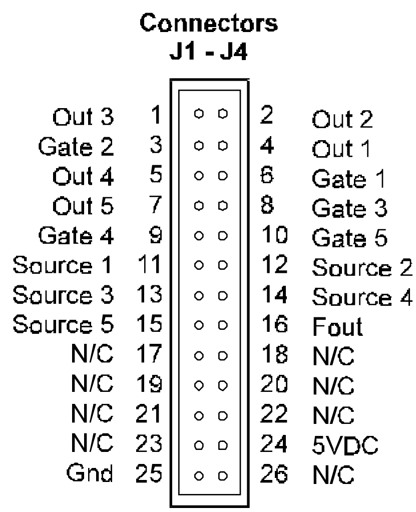


Figure 5-1: DCC5-P 37-Pin Connector

Counter and digital I/O signals are connected to the DCC10/20-P via a 26 Pin Connector.

Pin	Name	Function
1	OUT3	Digital Output Bit 3
2	OUT2	Digital Output Bit 2
3	GATE2	Counter 2 Gate
4	OUT1	Digital Output Bit 1
5	OUT4	Digital Output Bit 4
6	GATE1	Counter 1 Gate
7	OUT5	Digital Output Bit 5
8	GATE3	Counter 3 Gate
9	GATE4	Counter 4 Gate
10	GATE5	Counter 5 Gate
11	SOURCE1	Counter 1 Input
12	SOURCE2	Counter 2 Input
13	SOURCE3	Counter 3 Input
14	SOURCE4	Counter 4 Input
15	SOURCE5	Counter 5 Input
16	FOUT	Frequency Output
17	N/C	
18	N/C	
19	N/C	
20	N/C	
21	N/C	
22	N/C	
23	N/C	
24	+5VDC	+5 Volt Power (ref. only)
25	GND	Ground
26	N/C	



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Appendix A: LSI Type 9513 Data Sheet

The following pages contain the data sheet for the LSI Counter used on the DCC-P Series Counter Boards.

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Declaration of Conformity

(according to ISO/IEC Guide 22 and EN 45014)

INDUSTRIAL COMPUTER SOURCE®

6260 Sequence Drive
San Diego, CA 92121-4371
(800) 523-2320

declares, that the product:

DCC5-P DCC10-P DCC20-P

to which this declaration relates, meets the essential health and safety requirements and is in conformity with the relevant EU Directives listed below:

EU EMC Directive 89/336/EEC
EU Low Voltage Directive 72/23/EEC

using the relevant section of the following EU standards and other normative documents:

EN 50081-1:1992 Emissions, Generic Requirements.
-EN 55022 Measurement of radio interference charateristics of information technology equipment.

EN 50082-2:1995 Immunity, Generic Requirements.
-EN 61000-4-2 Immunity to Electrostatic Discharge.
-ENV 50140 Immunity for radiated RF electromagnetic fields.

EN 50082-1:1992 Immunity, Generic Requirements.
-IEC 801-3:1984 Immunity for radiated electromagnetic fields.
-IEC 801-4:1988 Immunity for AC and I/O lines, fast transient common mode.
-IEC 65A/77B Immunity for AC lines, transients, common, and differential mode.

EN 60950:1992 Safety of Information Technology Equipment.

September 17, 1997
San Diego, CA

Mr. Steven R. Peltier
President & Chief Executive Officer

Information supporting this declaration is contained in the applicable Technical Construction file available from:

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